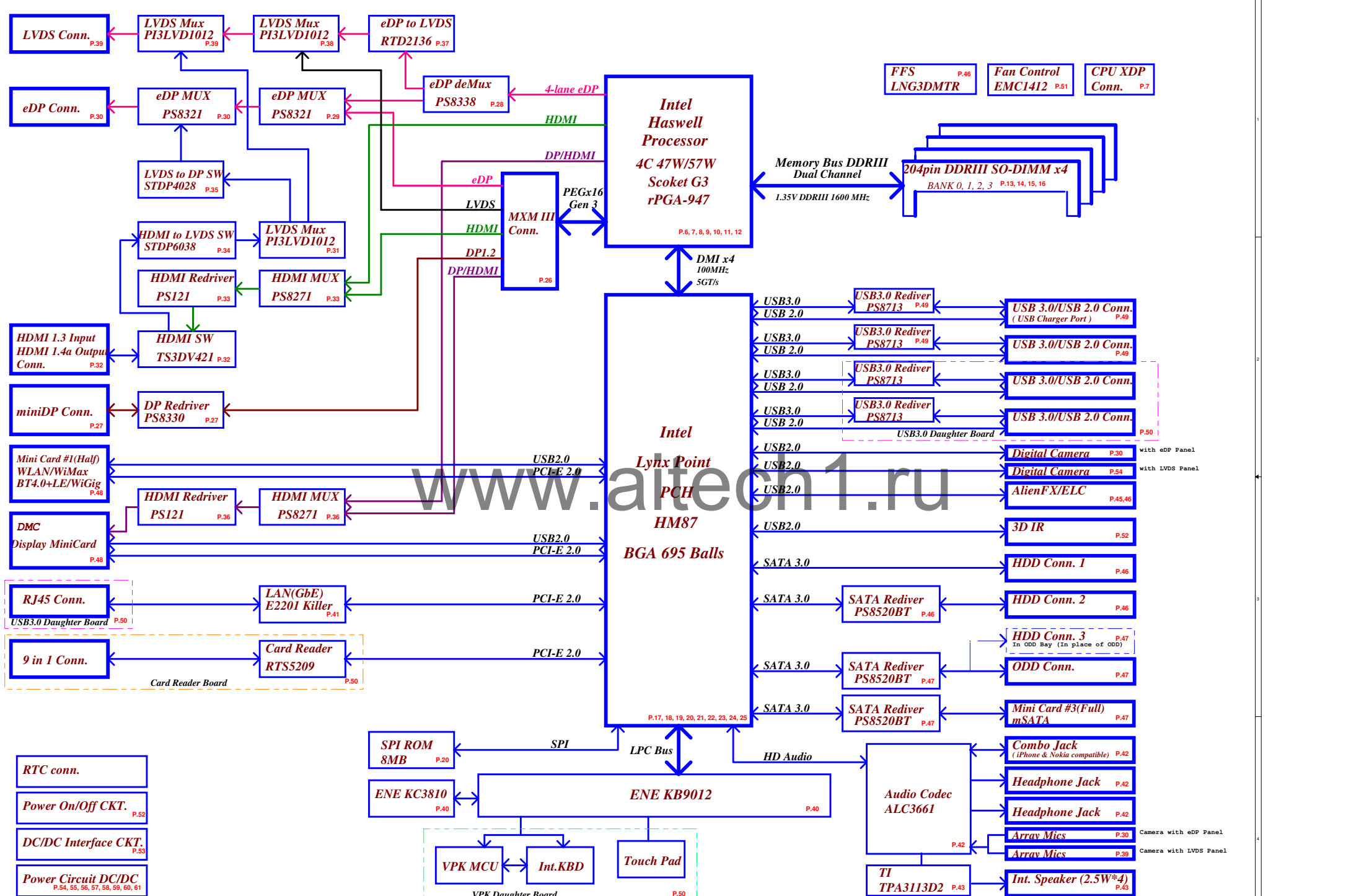


MODEL NAME : *RANGER 17*
PCB NO : *LA-9331P*
BOM P/N : *4619KL31L01*

Compal Confidential
RANGER 17
Schematic Document
Rev: X00
2012-06-22
@ : Nopop Component

Security Classification		Compal Secret Data		Title	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	Compal Electronics, Inc.	
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				LA-9331P	0.1
Date: Friday, June 22, 2012		Sheet 1 of 61			



Compal Confidential

Project Code : VAS00
File Name : LA-9331P

LS-9335P
POWER BUTTON/B

on/off SW

Led x 2

Hot Bar

LS-9336P
INDICATOR/B

Led-HDD

Led-Wireless

Led-CapsLock

Lid

FFC
20 pin

LS-9337P
CardReader /B

Card Slot

FFC
30 pin

LA-9331P M/B

22 pin
HDD2 conn.

50pin
B To B conn.

44 pin

20 pin

22 pin
HDD1 conn.

Camera

LCD Panel

Coaxial/Wire Combo

ODD /HDD3

LF-XXXXP
FPC

HDD in ODD Bay Cable

VPK Keyboard

30 pin

40 pin

KSI/KSO

LS-9338P
VPK Daughter/B

VPK MCU

MAX7313

Hot Key

6 pin

10 pin

Key Pad

Backlight / 8 Pressure-sense Analog Signals

FFC
16 pin

Touch Pad

FFC
4 pin

L

R

LS-9334P
LOGO /B

Led x 2

LS-9333P
Alien Slits-R Light/B

Led x 2

LS-9331P
Alien head badge/B

Led x 2

LS-9332P
Alien Slits-L Light/B

Led x 2

LS-9339P
USB30 /B

50pin
B To B conn.

RJ45

USB3.0

USB3.0

Tron Light

To M/B

Wire
6pin

LS-933BP
Tron L/B

Led x 1

To M/B

Wire
10pin

LS-933DP
Tron FL/B

Led x 1

LS-933EP
Tron FR/B

Led x 1

To USB30/B

Wire
6pin

LS-933CP
Tron R/B

Led x 1

Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1 (SSI)
1	0.2 (PT)
2	0.3 (ST)
3	0.4 (QT)
4	1.0 (MP)
5	
6	
7	

USB 3.0 PORT	Connction
1	JUSB1 (Left side)
2	JUSB2 (Left side)
3	NA
4	NA
5	JUSB3 (Right side)
6	JUSB4 (Right side)

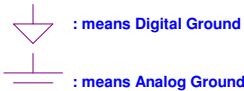
POWER STATES

State	Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0		HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF		LOW	HIGH		HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF		LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF		LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

State	power plane	+5VALW +3VALW +3VLP +3V_PCH	+1.35V +1.05V	+5VS +3VS +1.5VS +1.05VS +0.675VS +3VMXM +5VMXM +VCC_CORE +1.35V_CPU_VDDQ
S0		ON	ON	ON
S3		ON	ON	OFF
S5 S4/AC		ON	OFF	OFF
S5 S4/AC don't exist		OFF	OFF	OFF

Symbol Note :



CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	MINI CARD-1 WLAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD-2 DMC	CLKOUTFLEX1	None
	CLKOUT_PCIE2	10/100/1G LAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	CARD READER	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_A	MXM		

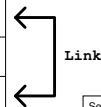
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	80port debug card
PCI3	None
PCI4	None

SATAIII	DESTINATION
SATA0	HDD1
SATA1	HDD2
SATA2	ODD
SATA3	mSATA
SATA4/PCIE LANE1	MINI CARD-1 WLAN
SATA5/PCIE LANE2	MINI CARD-2 DMC

PCI EXPRESS	DESTINATION
Lane 1/USB3.0 Port 3	None
Lane 2/USB3.0 Port 4	None
Lane 3	10/100/1G LAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

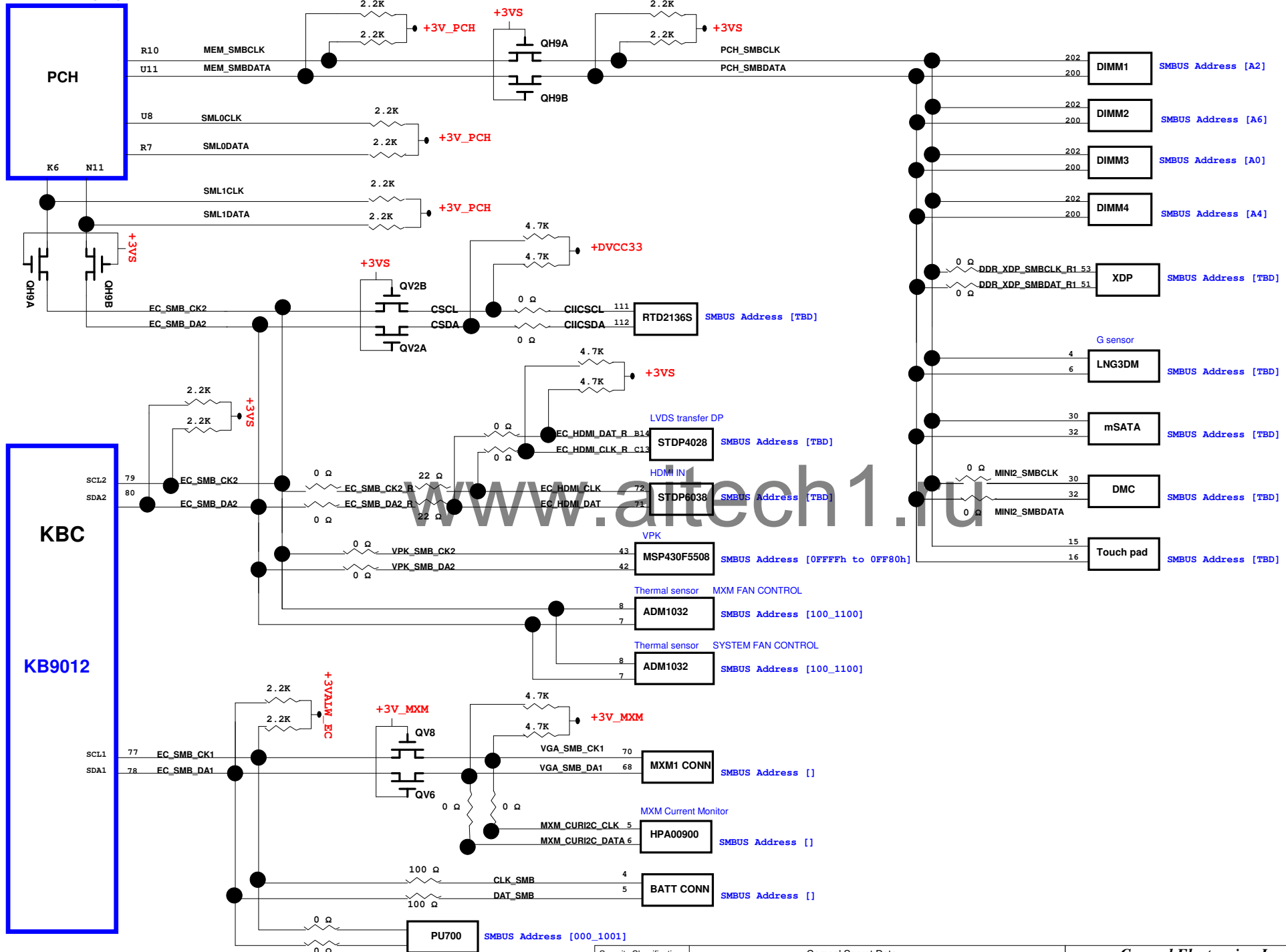
SMBUS Control Table

	SOURCE	WLAN	DMC	BATT	DIMM	6038	4028	Thermal Sensor	FFS	2136	VPK MCU	MXM	XDP	Charger	TP	mSATA
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V		V		
EC_SMB_CK2 EC_SMB_DA2	KB9012					V	V	V		V	V					
PCH_SMLCLK PCH_SML0DATA	PCH															
PCH_SML1CLK PCH_SML1DATA	PCH															
MEM_SMBCLK MEM_SMBDATA	PCH		V		V				V				V	V	V	V

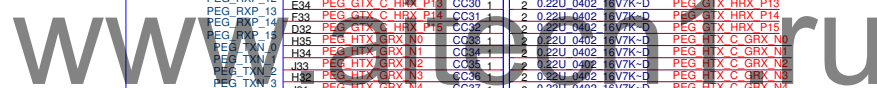
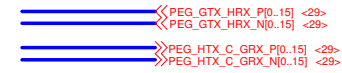


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				Date	Friday, June 22, 2012
				Sheet	4 of 61

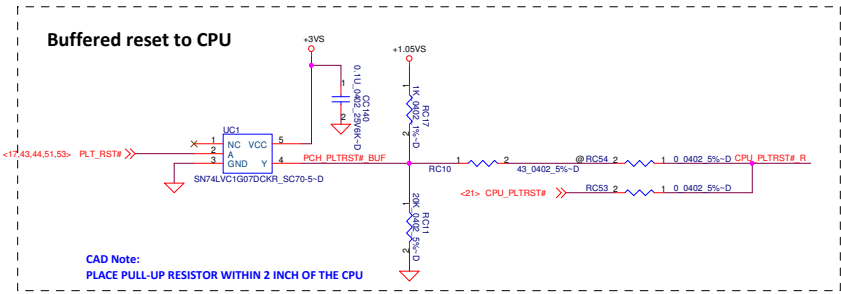
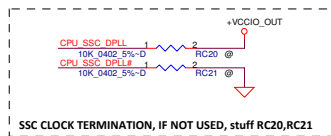
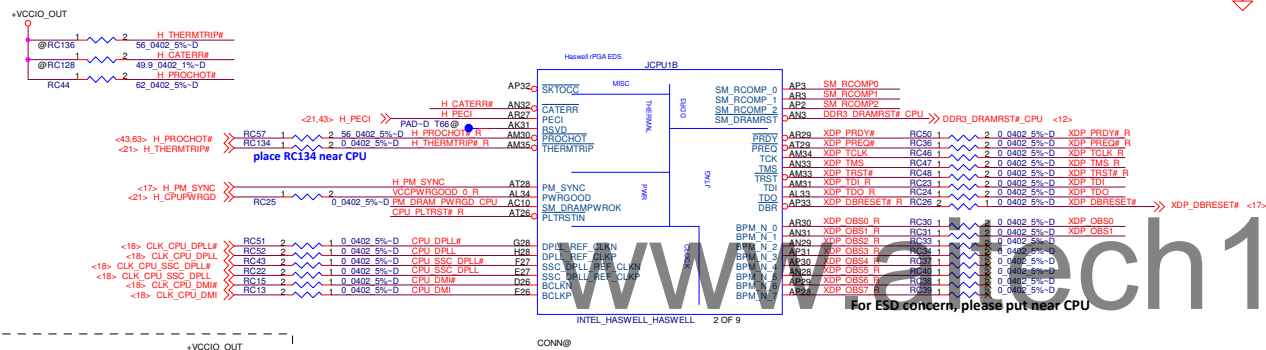
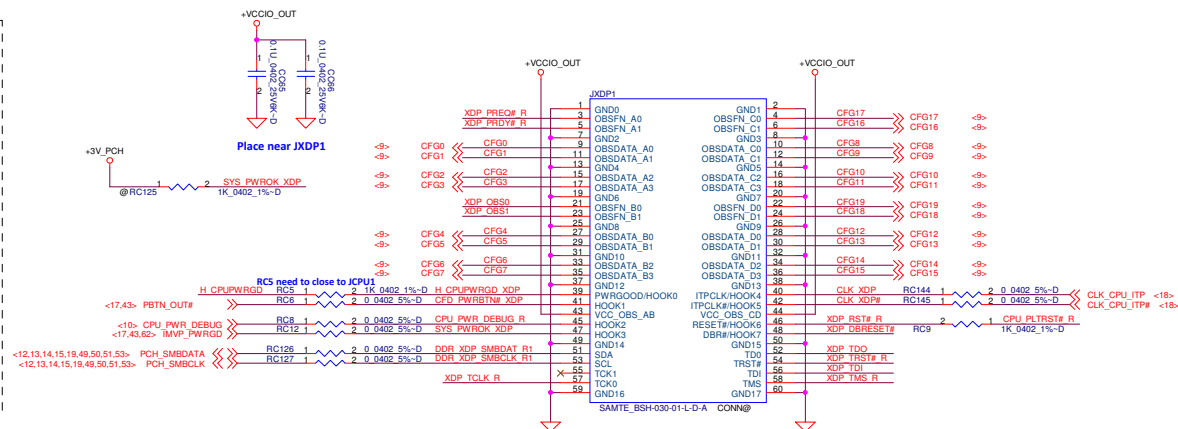
SMBUS Address [TBD]



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Size		Document Number		Rev	
Custom		LA-9331P		0.1	
Date		Friday, June 22, 2012		Sheet 5 of 61	



Rev	0.1
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CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC25 & RC130

DDR3 COMPENSATION SIGNALS

SM_RCMP0 RC45 1 2 100 0402 1%-D

SM_RCMP1 RC55 1 2 75 0402 1%-D

SM_RCMP2 RC49 1 2 100 0402 1%-D

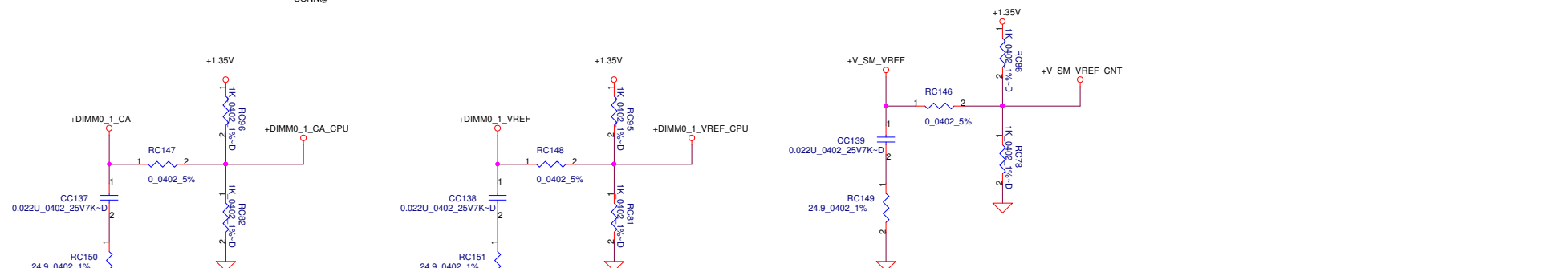
CAD Note:
 Trace width=12~15 mil, Spacing=20 mils
 Max trace length= 500 mil

PU/PD for JTAG signals

The diagram illustrates the power-up/pull-down (PU/PD) configuration for JTAG signals. It shows a 3V5 supply connected to the top of the circuit. A 1.05V5 supply is connected to the bottom of the circuit. The signals and their connections are as follows:

- XDP DBRESET#**: Connected to **RC19 2** with a pull-up resistor to 3V5.
- XDP TMS**: Connected to **RC27 2** with a pull-up resistor to 1.05V5.
- XDP TDI_R**: Connected to **RC29 2** with a pull-up resistor to 1.05V5.
- XDP-PROG#**: Connected to **RC32 2** with a pull-up resistor to 1.05V5.
- XDP TDO_R**: Connected to **RC35 2** with a pull-up resistor to 1.05V5.
- XDP TCLK**: Connected to **RC42 2** with a pull-up resistor to 1.05V5.
- XDP TRST#**: Connected to **RC41 2** with a pull-down resistor to ground.

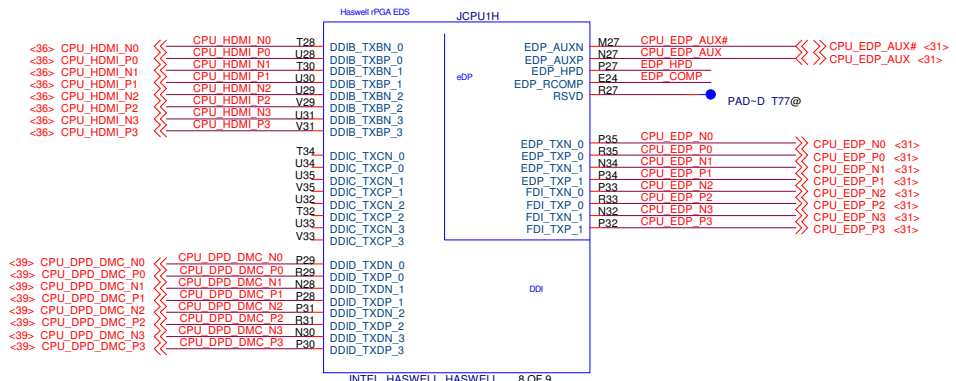
Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	Docu- ment Number	CPU (2/7) PM.XDP.CLK	
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Date	Friday, June 22, 2012		Sheet	7 of 61		



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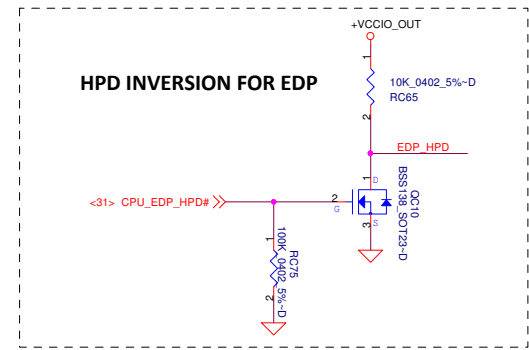
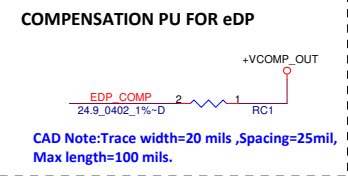
HDMI

DMC

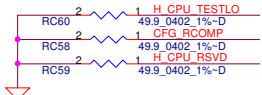


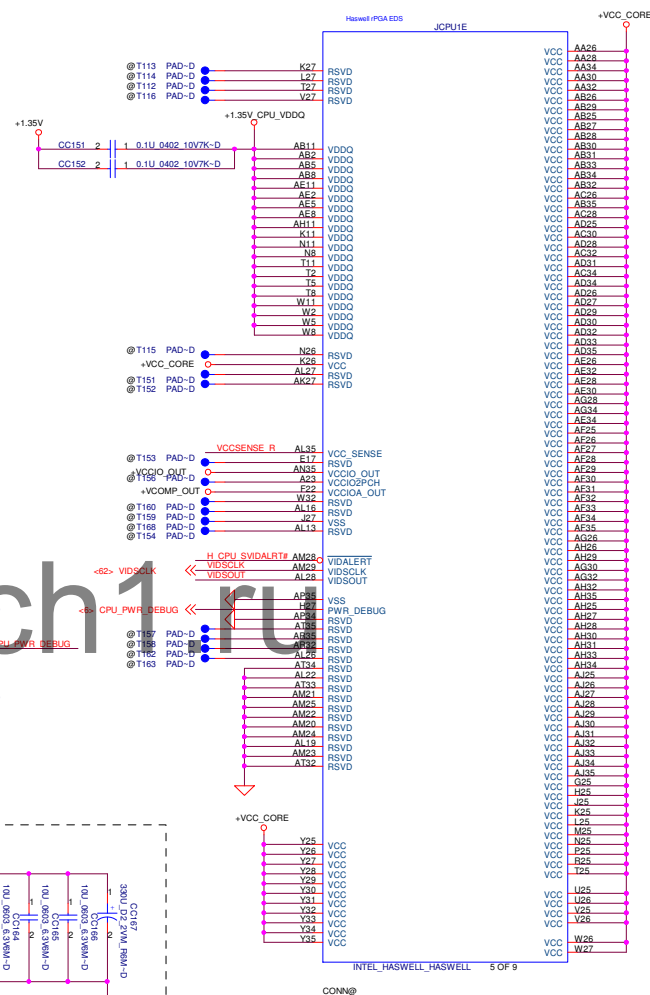
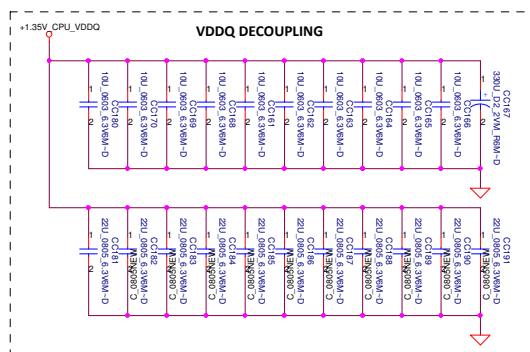
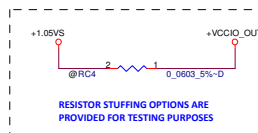
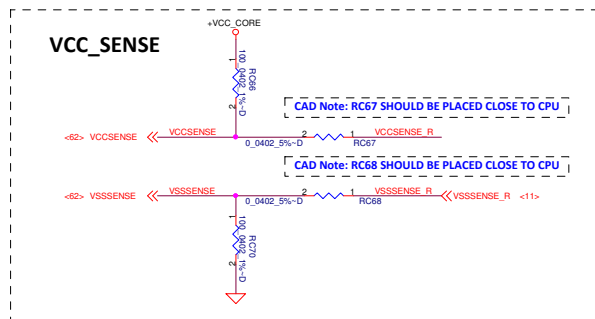
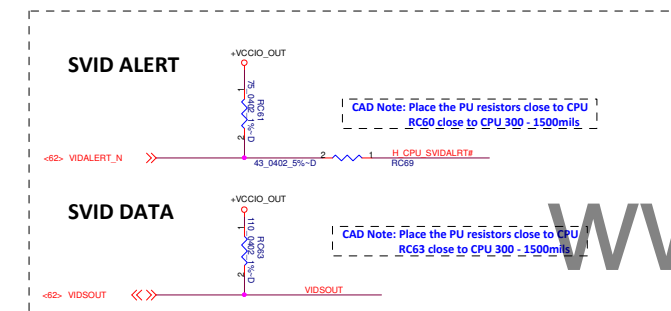
CONN@

www.aitech1.ru

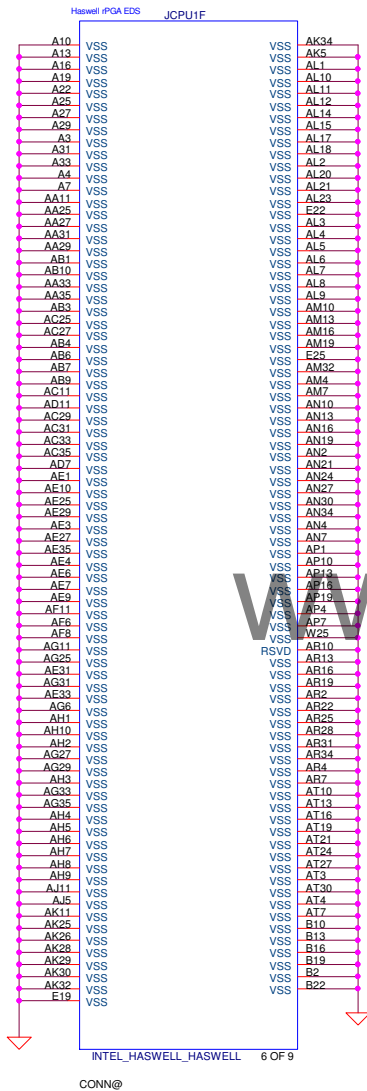


A circuit diagram showing a 1k resistor with 0.02% tolerance and 1% derating factor (1K 0A02 1%-D) connected to a CFG7 signal source. The resistor is connected in series with the signal source, and its terminals are labeled 1 and 2.



[illegible]

Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> Title CPU (6/7) PWR	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	Doc Number LA-933IP	Rev 0.1
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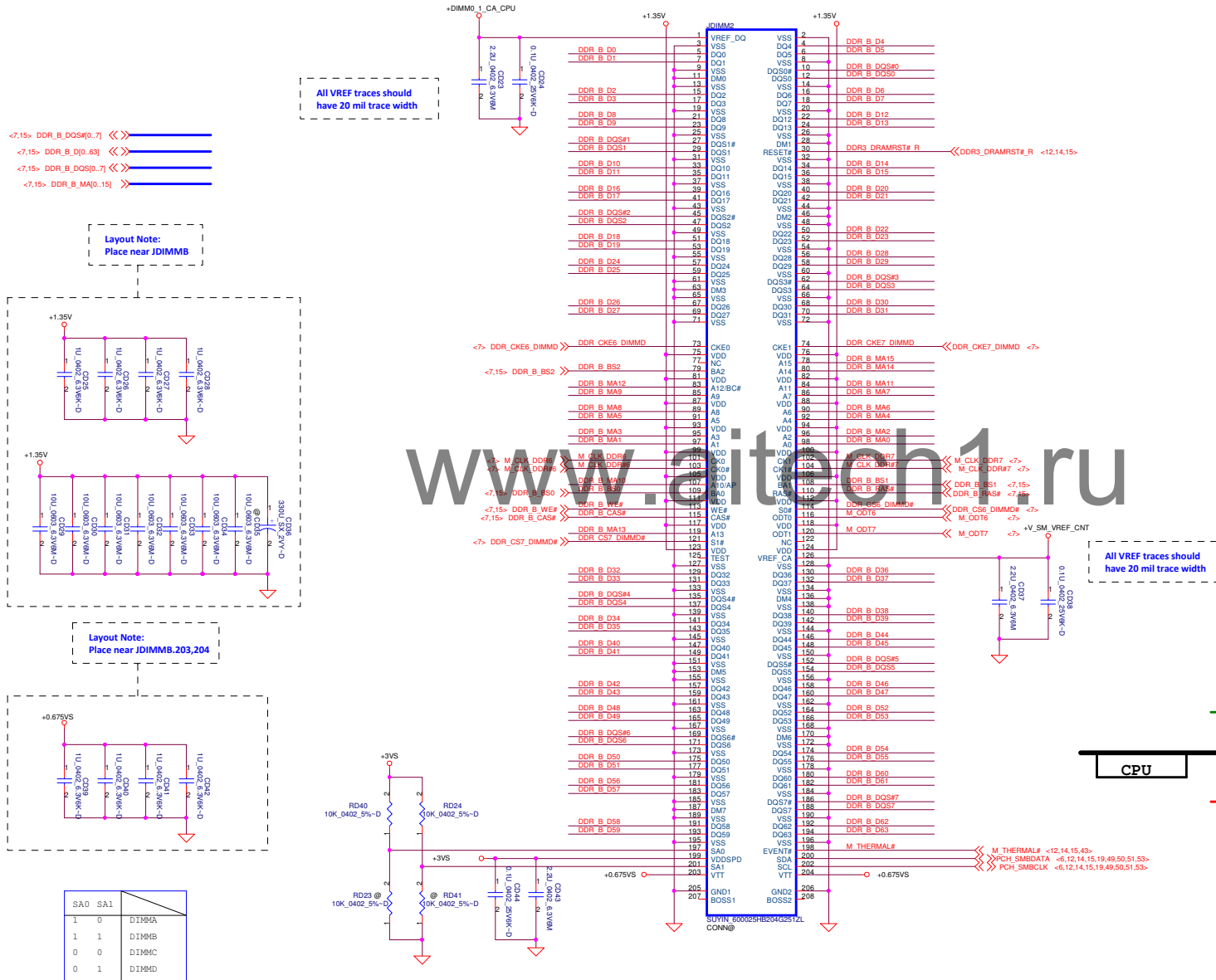




SA0	SA1	
1	0	DIMM1A
1	1	DIMM1B
0	0	DIMM2C
0	1	DIMM2D

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				Doc Title	LA-9331P	
				Doc Date	Friday, June 22, 2012	
				Sheet	13	of 61

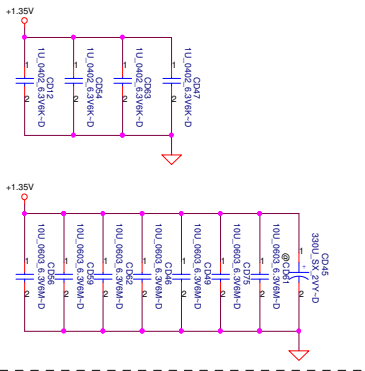
JDIMMB H=4mm



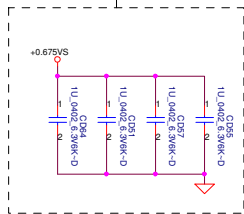
JDIMMC H=5.2mm

<7,12> DDR_A_DQS[0..7] <>
 <7,12> DDR_A_D[0..63] <>
 <7,12> DDR_A_DQS[0..7] <>
 <7,12> DDR_A_MA[0..15] <>

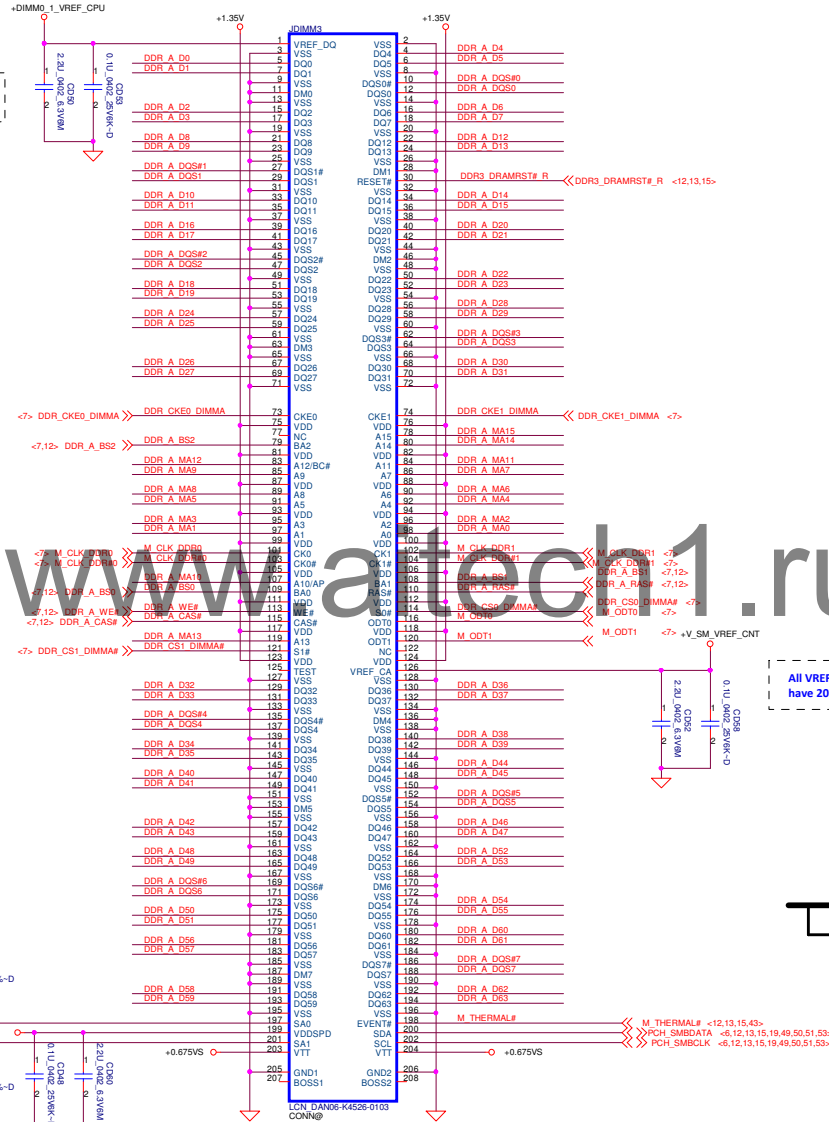
Layout Note:
Place near JDIMMC



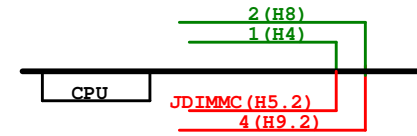
Layout Note:
Place near JDIMMC.203,204



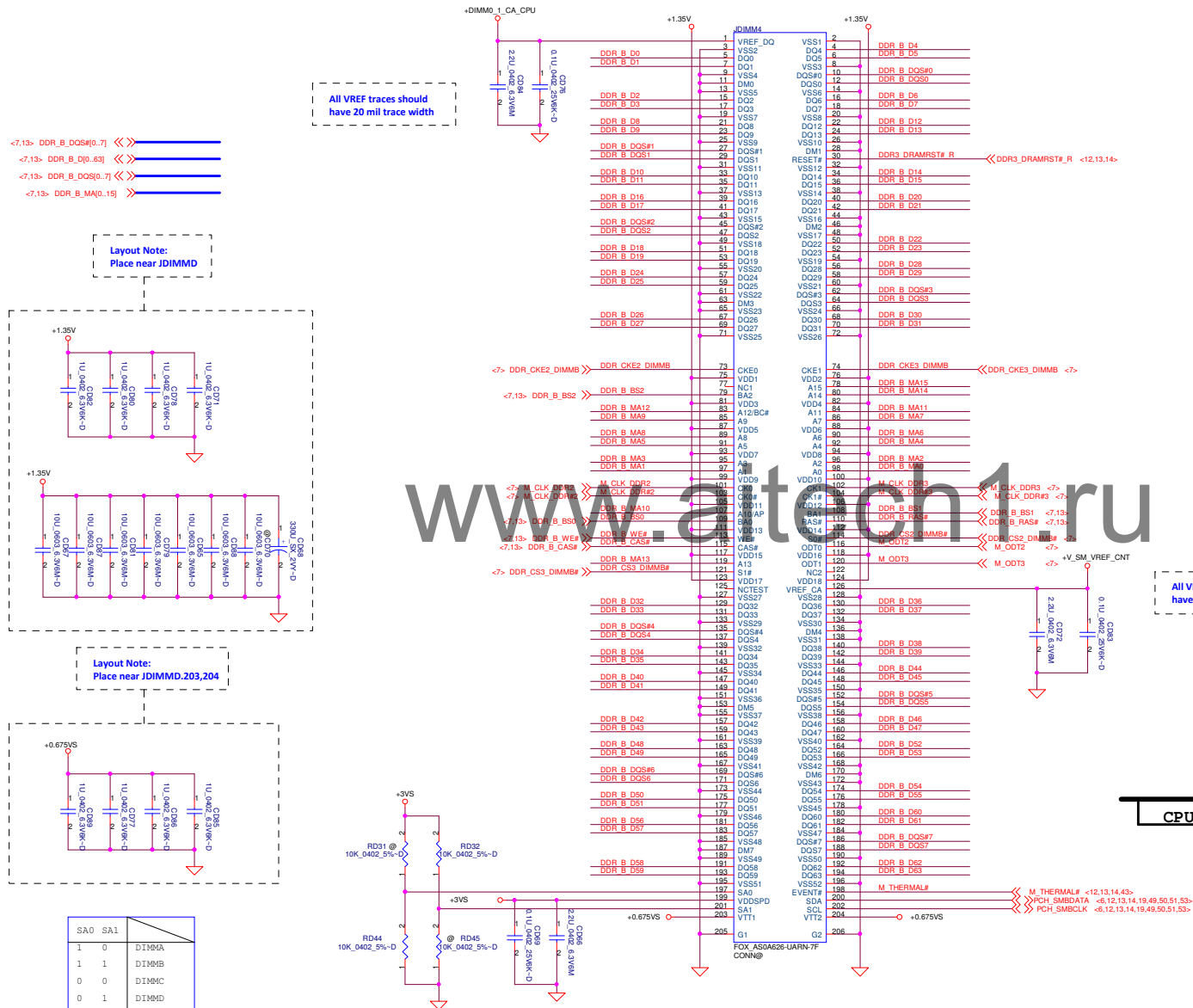
SA0	SA1	
1	0	DIMMA
1	1	DIMMB
0	0	DIMMC
0	1	DIMMD



All VREF traces should
have 20 mil trace width

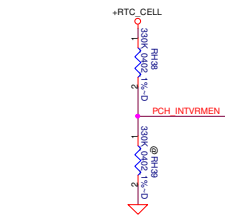


JDIMMD H=9.2mm

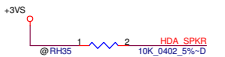


SA0	SA1	
1	0	DIMMA
1	1	DIMMB
0	0	DIMMC
0	1	DIMMD

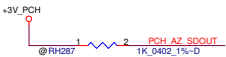
Security Classification	Compal Secret Data			Compal Electronics, Inc. DDRIII DIMMID	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	Title	
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				Date: Friday, June 22, 2012	Sheet 16 of 61



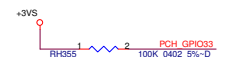
INTVRMEN - INTEGRATED SUS 1.05V VRM
ENABLE
High - Enable Internal VRs
Low - Enable External VRs



NO REBOOT STRAP
DISABLED WHEN LOW (DEFAULT)
ENABLED WHEN HIGH



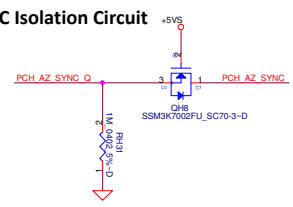
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED



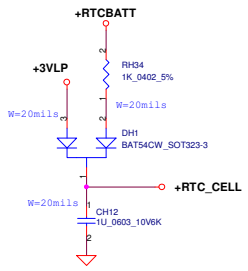
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

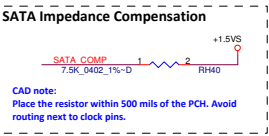
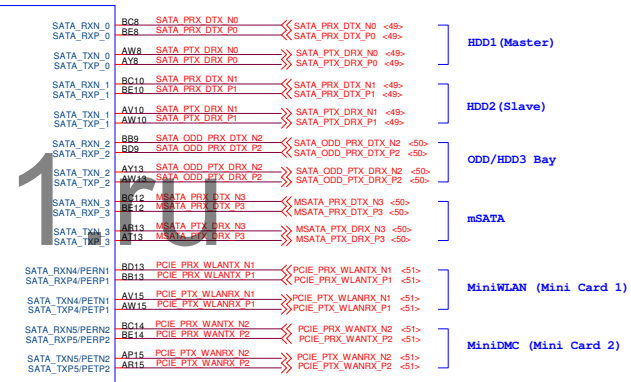
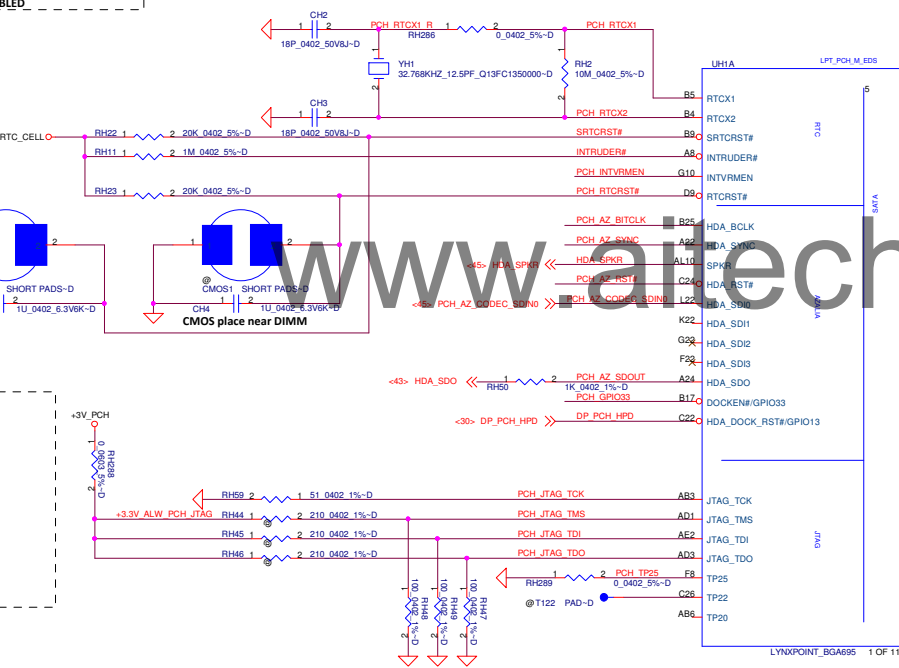
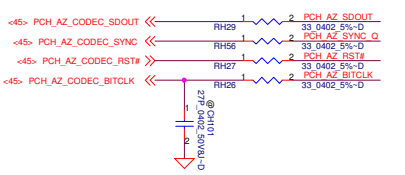
HDA_SYNC Isolation Circuit



RTC Battery

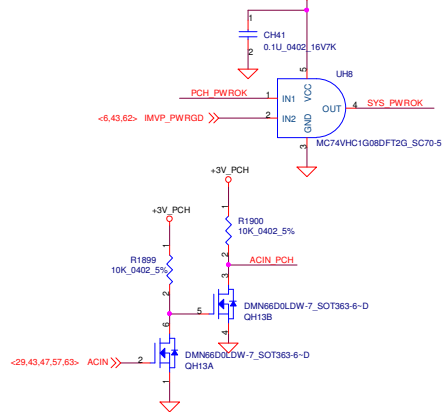
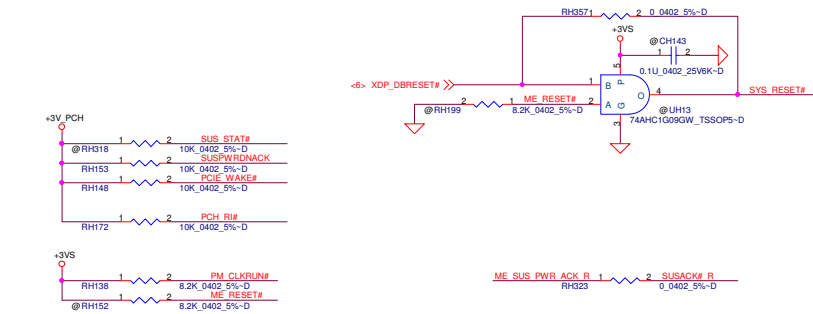


HDA for Codec



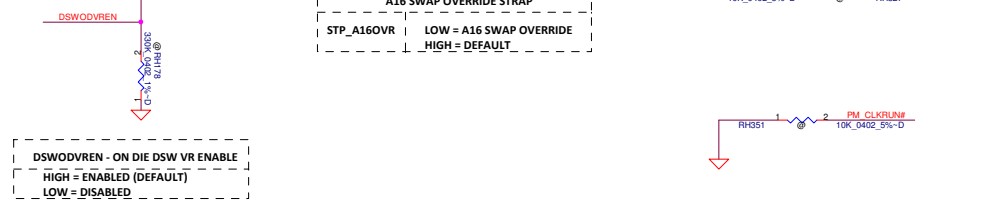
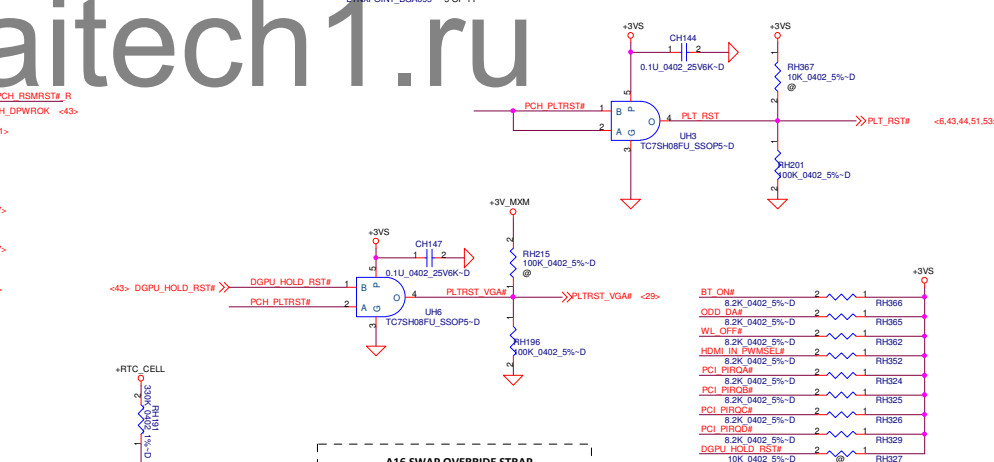
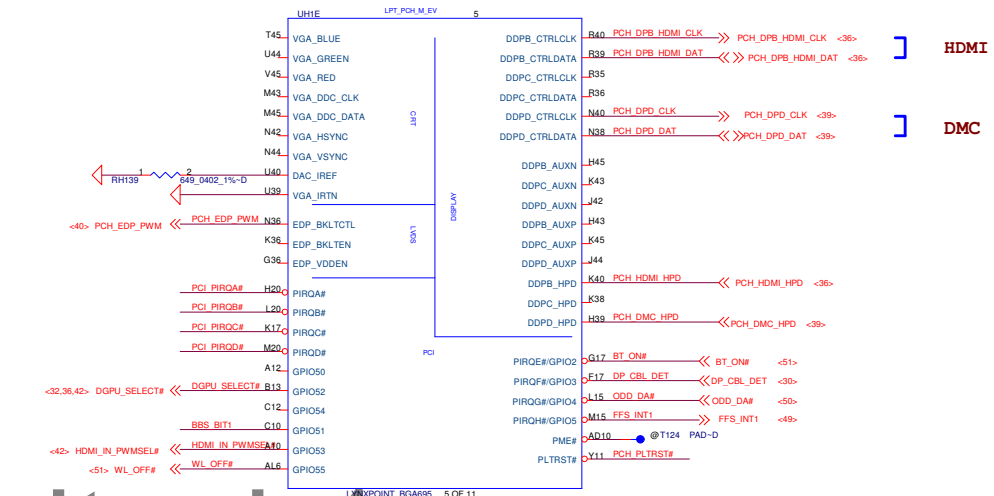
CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

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Issued Date	2012/06/22	Deciphered Date
2013/06/21		
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Date	Friday, June 22, 2012	Sheet 17 of 61

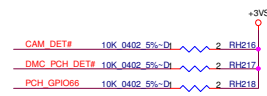
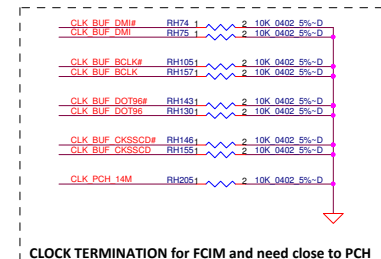


Boot BIOS Strap		
GNT1#/GPIO1 (BBS_BIT1)	SATA1GP/GPIO19 (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

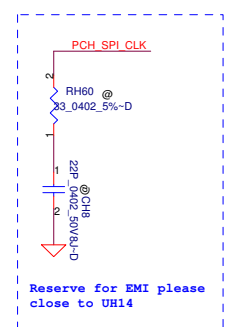
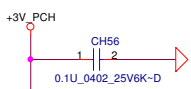
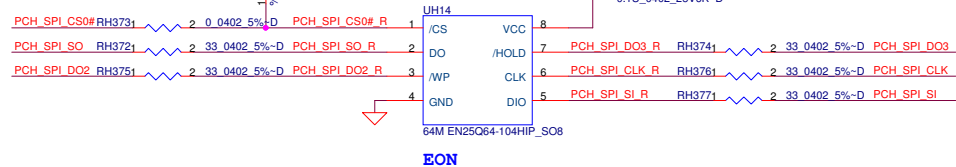
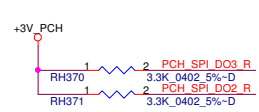
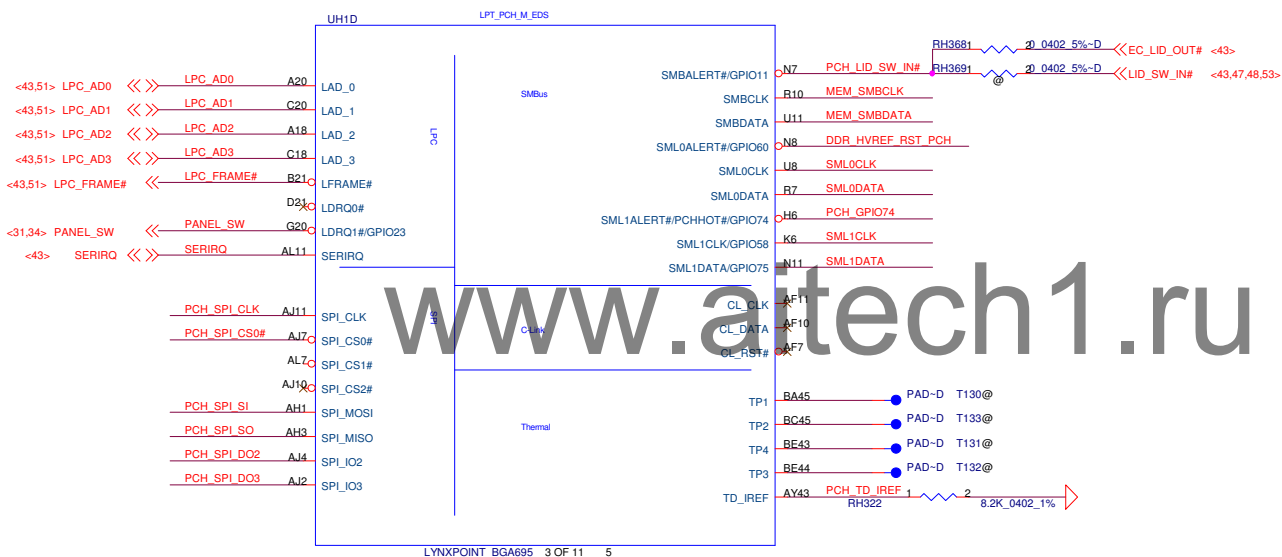
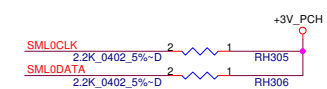
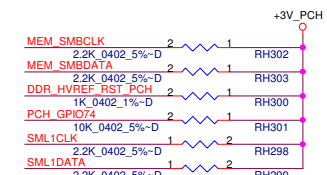
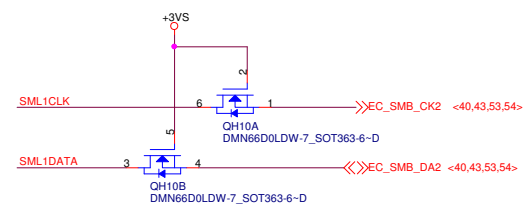
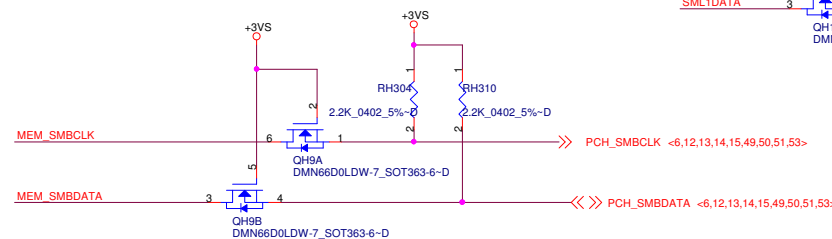
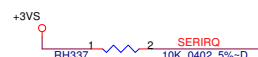
* GPIO51 has internal pull up.



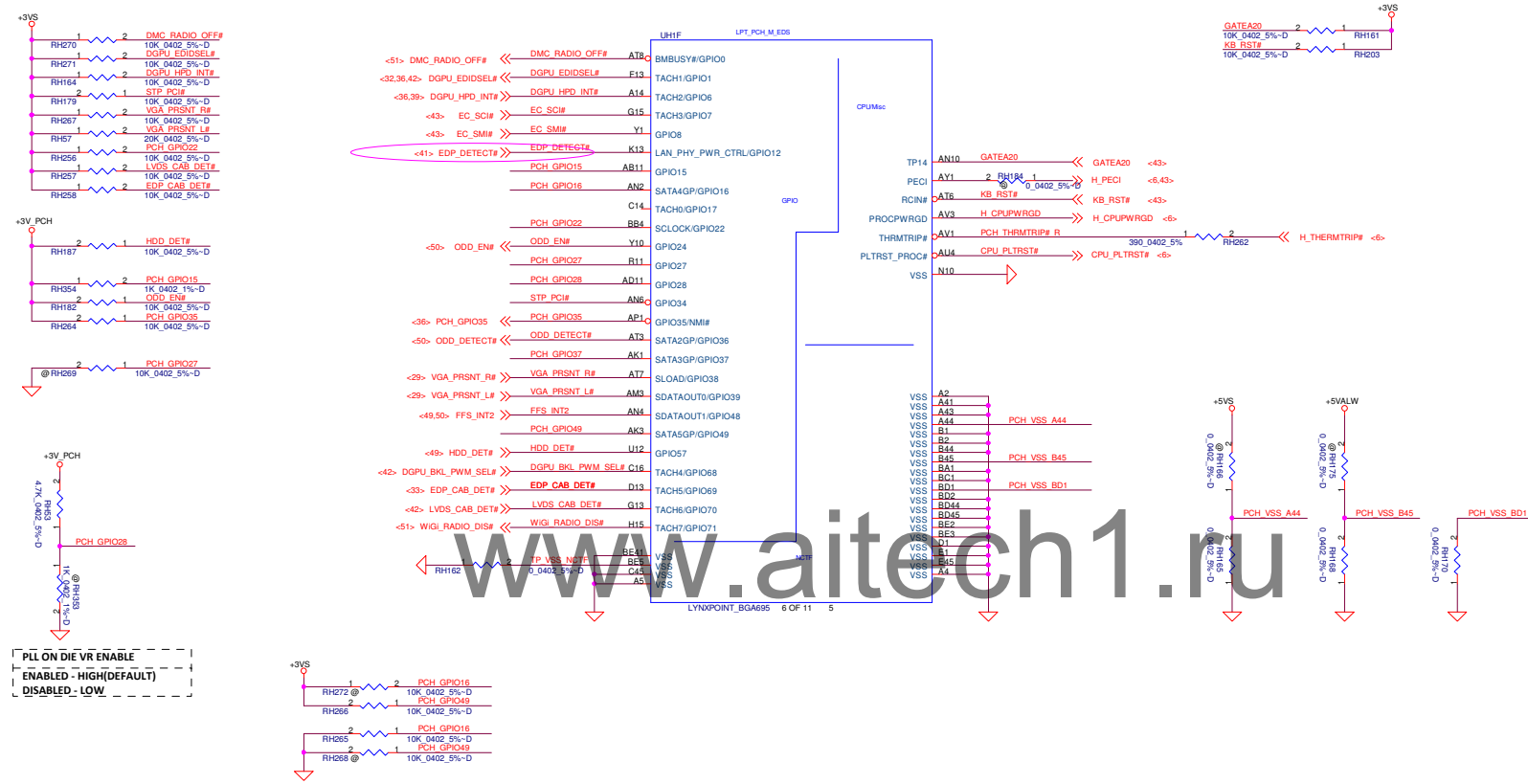
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Issued Date	2012/06/22	Deciphered Date	2013/06/21
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Sheet		18 of 61	



Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> PCH (3/9) CLK	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	Title FR-9331P	Document Number 19-01
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Security Classification		Compal Secret Data		Title	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	PCH (4/9) SPI, SMBUS, LPC	
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				LA-9331P	0.1
Date: Friday, June 22, 2012				Sheet	61



PLL ON DIE VR ENABLE
ENABLED - HIGH(DEFAULT)
DISABLED - LOW

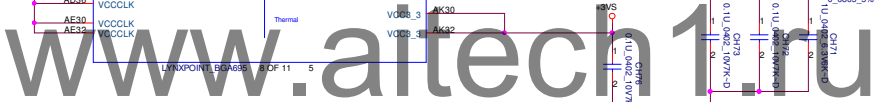
Config	GPIO16,49
USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01

Fixed Signals				Muxed Signals				Fixed Signals				Muxed Signals				Fixed Signals			
USB3_1	USB3_2	USB3_3	USB3_4	PCIE_1	PCIE_2	PCIE_3	PCIE_4	PCIE_5	PCIE_6	PCIE_7	PCIE_8	SATA_1	SATA_2	SATA_3	SATA_4	SATA_5	SATA_6	SATA_7	SATA_8
				(00)	(00)							(00)	(00)						
				USB3_3	USB3_4							PCIE_1	PCIE_2						
				(01)	(01)							(01)	(01)						

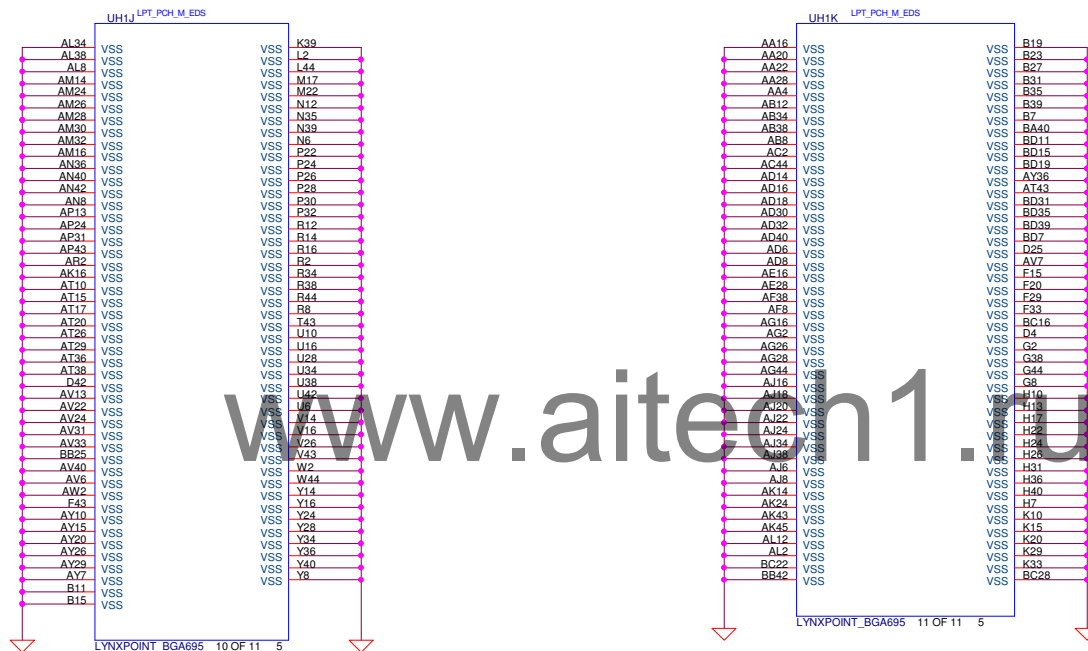
SATA2GP/GPIO36, SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK.
WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER PLRST_N DE-ASSERTS).
NOTE: THIS SIGNAL SHOULD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.



Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

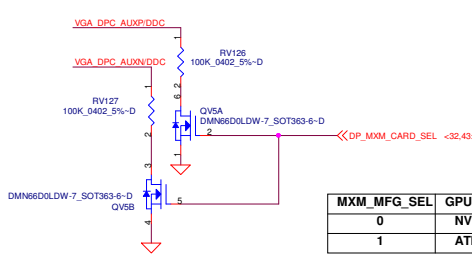
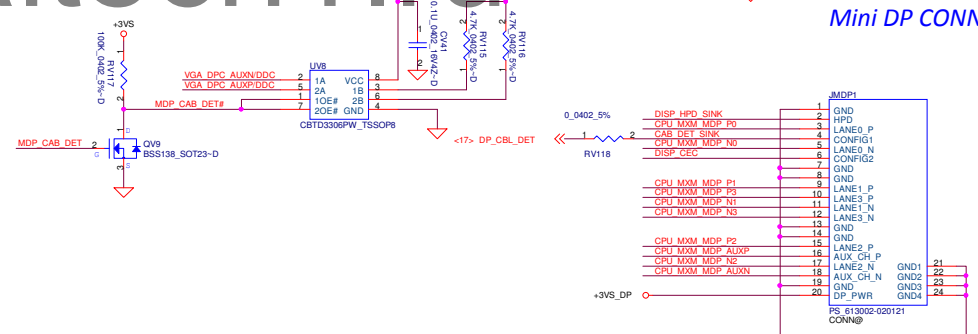
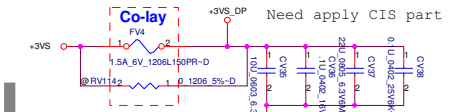
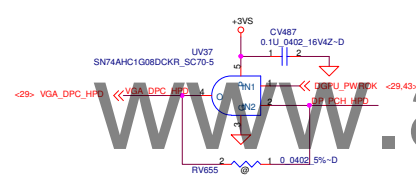
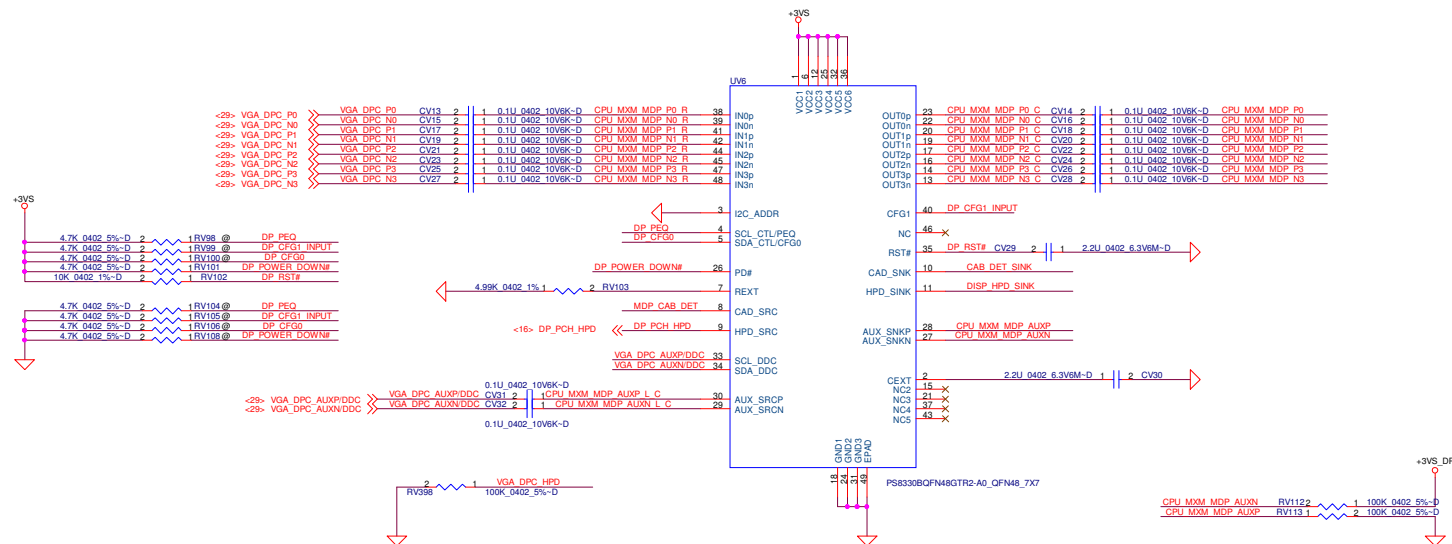


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Security Classification		Compal Secret Data		Title	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	PCH (9/9) Power	
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				LA-9331P	0.1
				Date: Friday, June 22, 2012	Sheet 25 of 61

DP Redriver



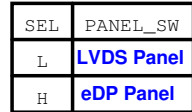
MXM_MFG_SEL	GPU Source
0	NVIDIA
1	ATI

Security Classification	Compal Secret Data		
Issued Date	2012/06/22	Deciphered Date	2013/06/21

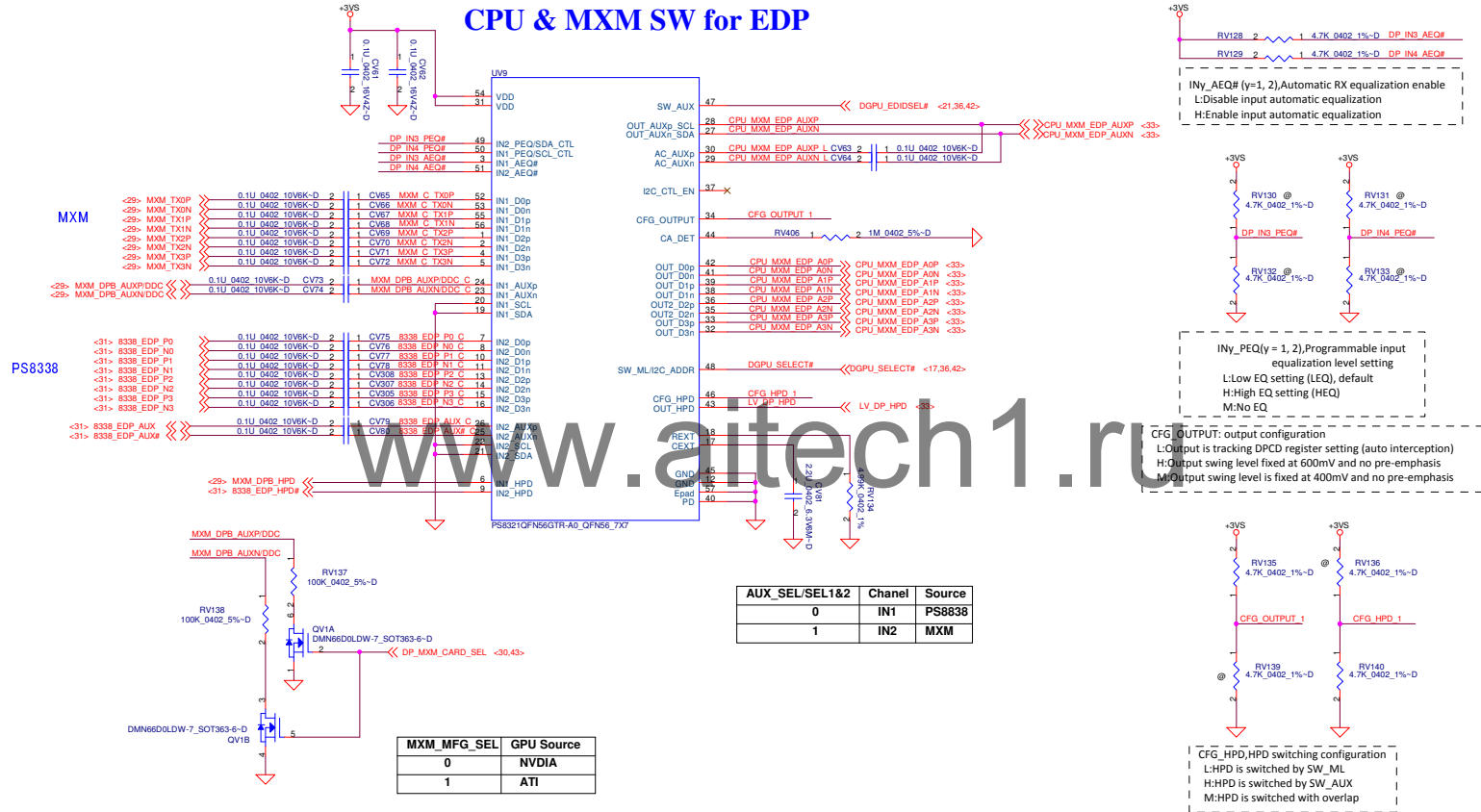
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Compal Electronics, Inc.			
Title			
Mini DP/Thunder Bolt power			
Rev A28	Document Number	Rev 0.1	
Custom	LA-9331P		
Date	Expiry	Sheet	of
2012	June 23 2012	27	64

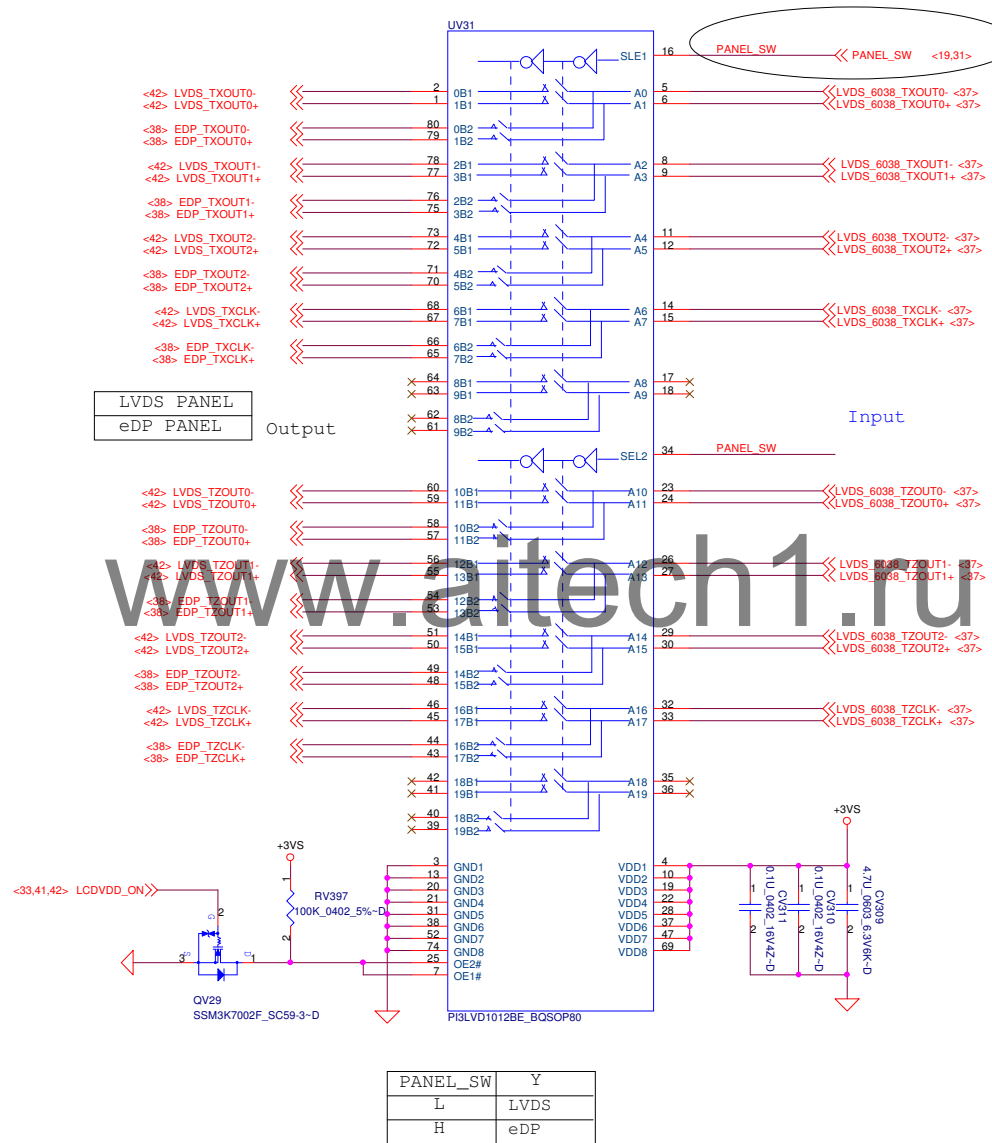
Pin 1 to 14 of the 8338 EDP HPD# pin header. The diagram shows connections for PC11, PC10, PC20, PC2, OUT2_CA_DET, OUT2_HP0, SW, PEO, PWDN, and PEX. It also shows a 1K 0402-5% resistor connected to the SW pin and a 1.1R RV416 resistor connected to the PWDN pin. The PWDN pin is also connected to a 3V3 supply.

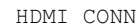


Security Classification		Compal Secret Data		Title			
Issued Date	2012/06/22	Deciphered Date	2013/06/21	CPU to EDP & LVDS MUX			
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				LA-9331P		0.1	
				Date	Friday, June 22, 2012	Sheet	28 of 61

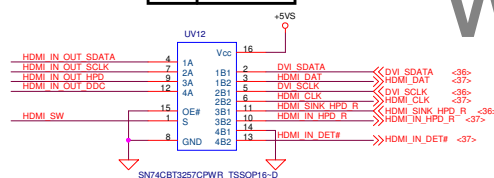


STDP6038 to EDP & LVDS MUX





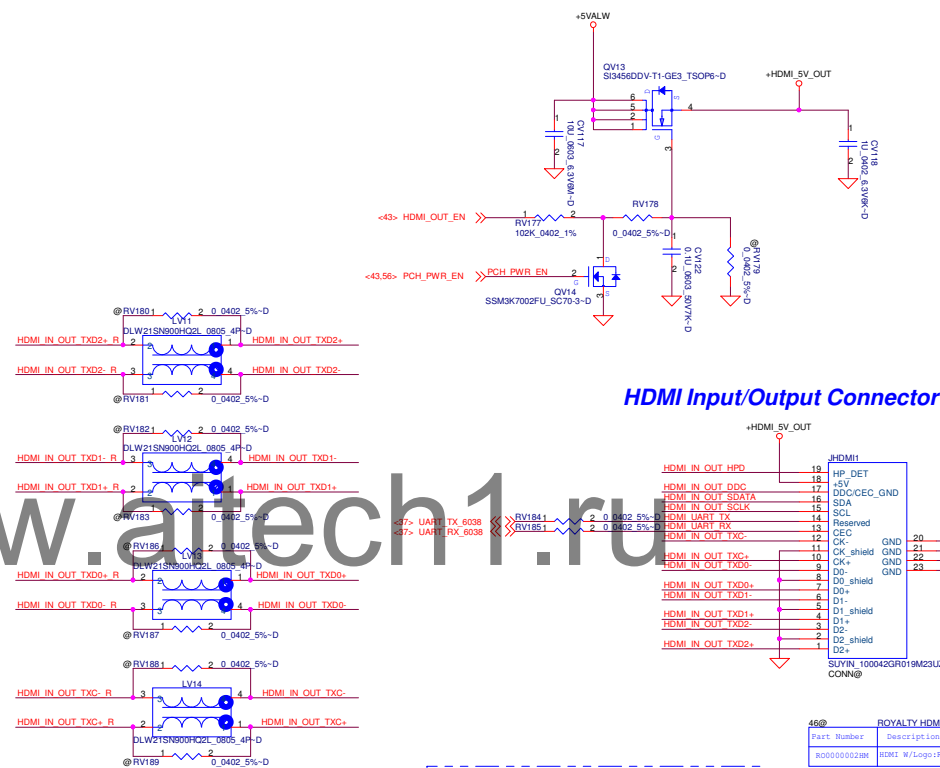
SEL	OUTPUT
L	A
H	B



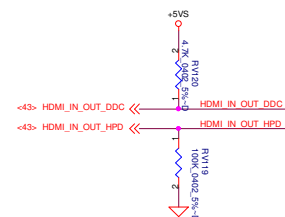
SEL	OUTPUT
L	B1
H	B2

STDP6038

CPU/MXM



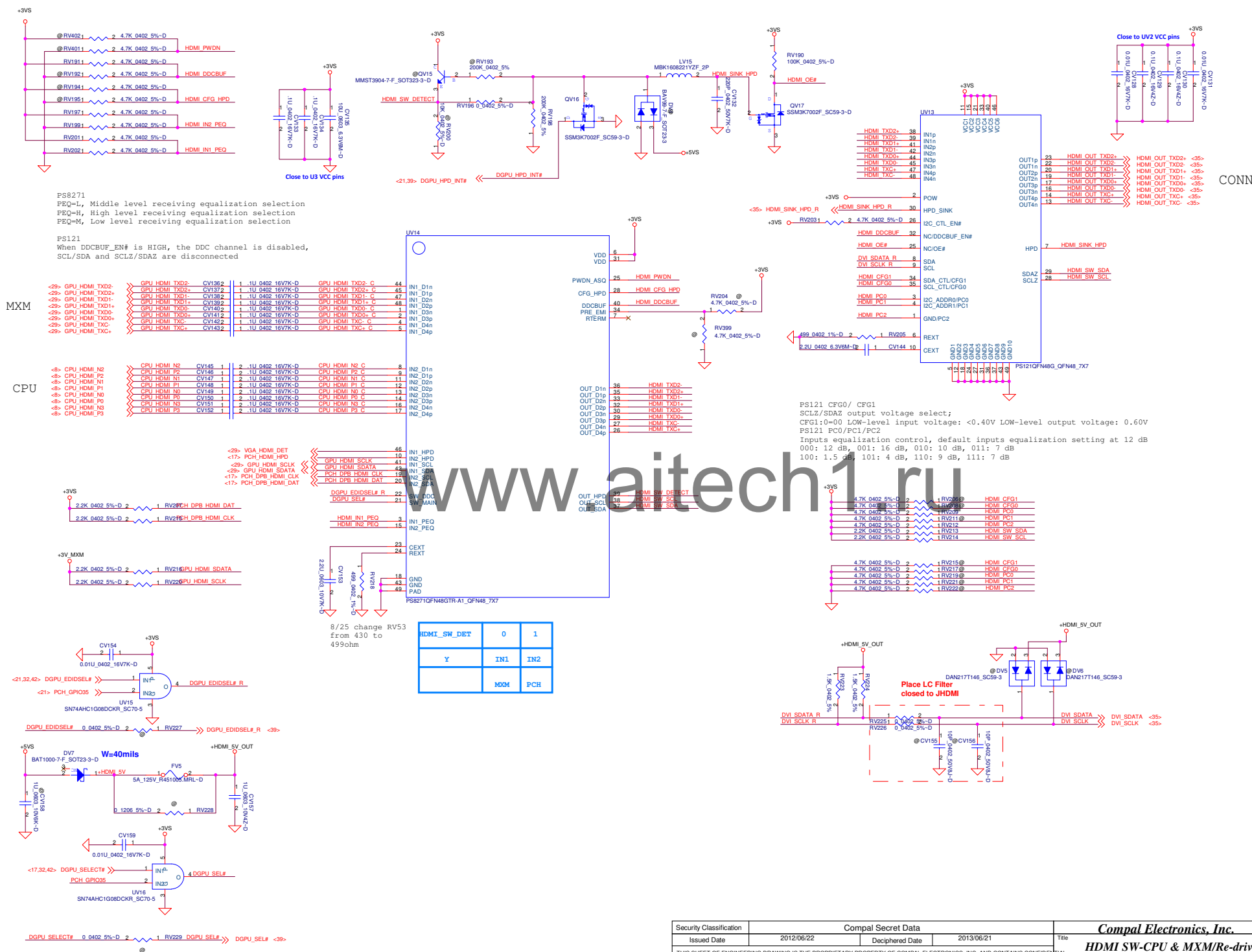
HDMI Input/Output Connector

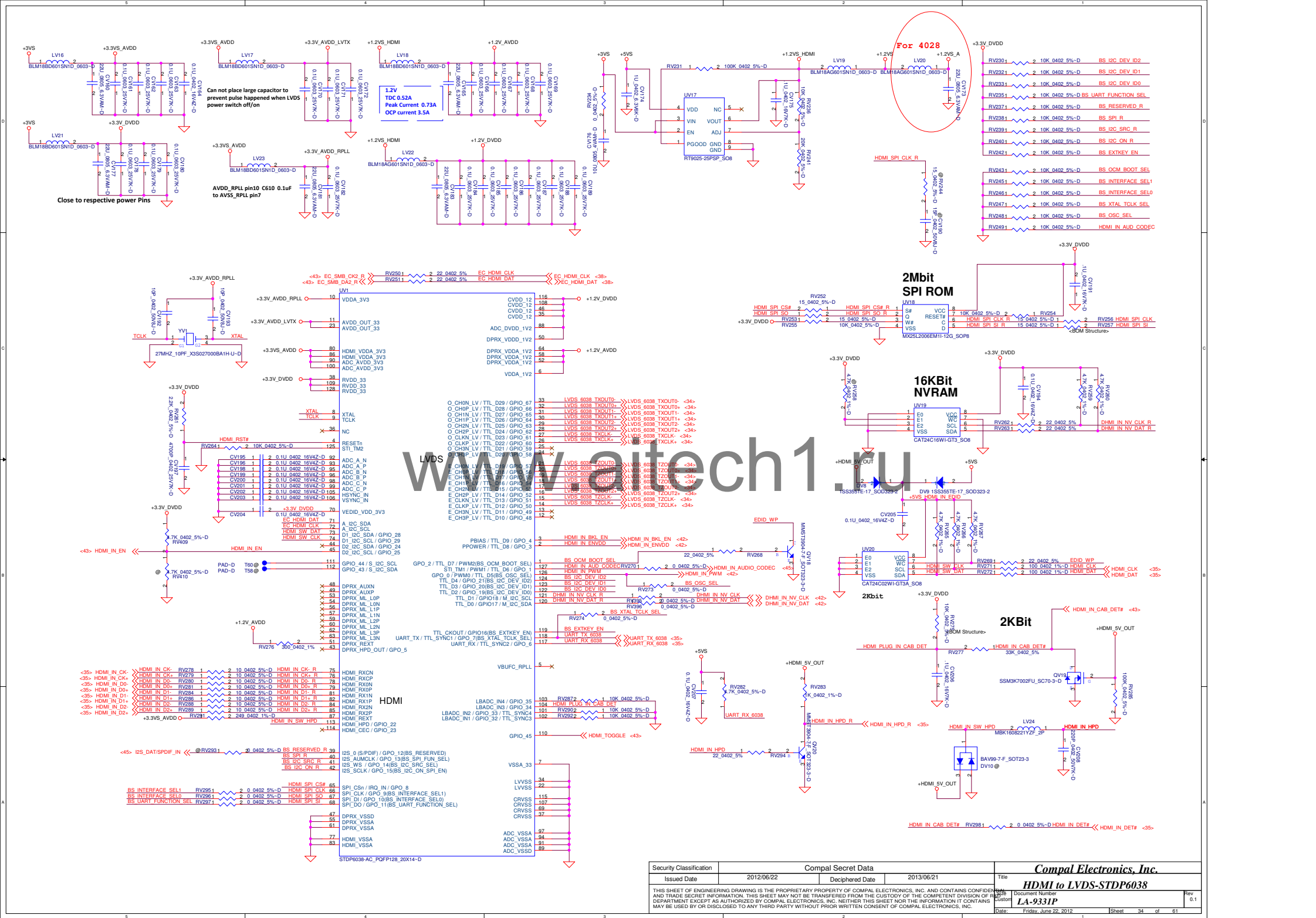


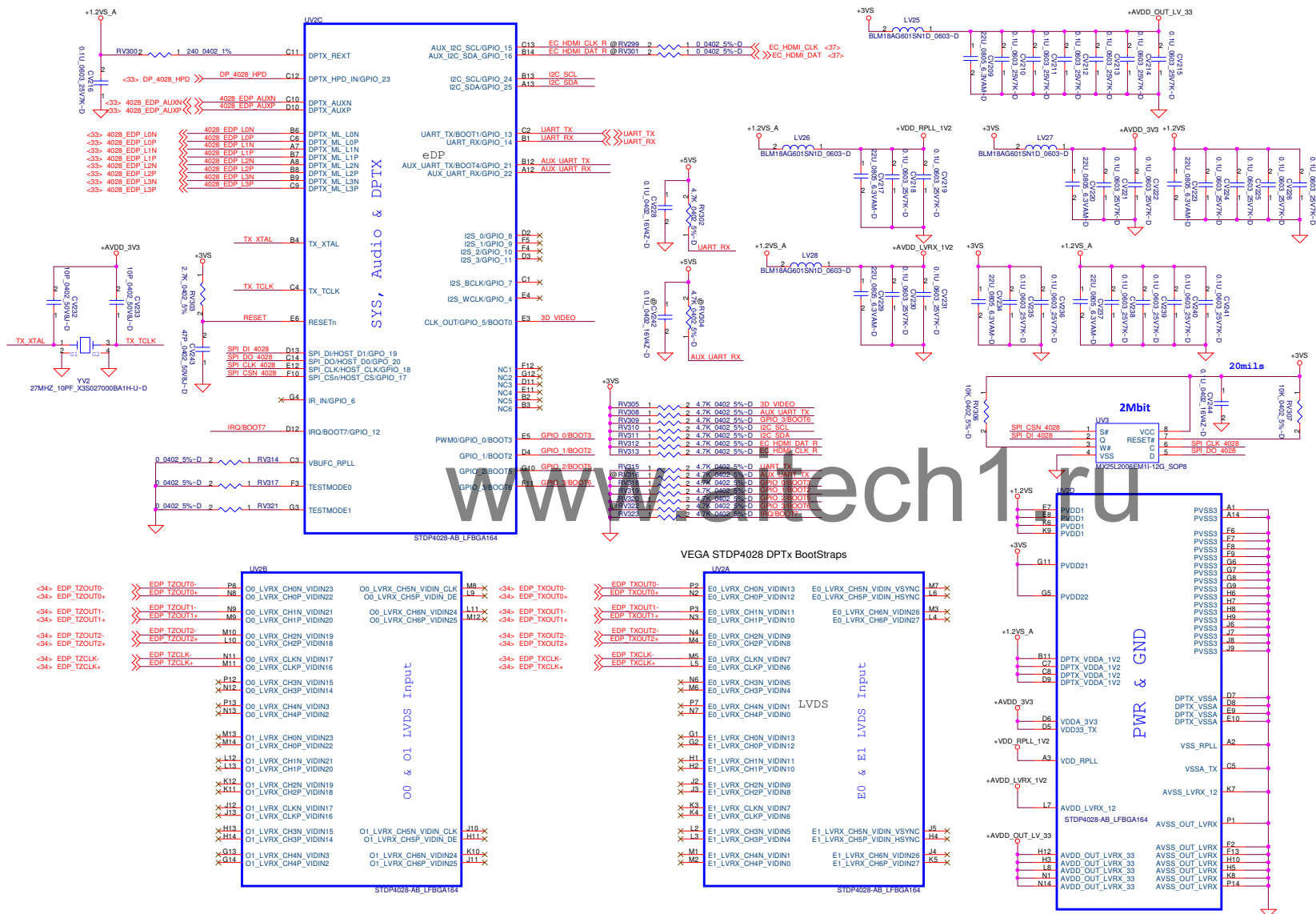
HDMI IN OUT TXC-	CV349	1	2	3.3P	0402	50V8C-D
HDMI IN OUT TXC+	CV350	1	2	3.3P	0402	50V8C-D
HDMI IN OUT TXD0-	CV351	1	2	3.3P	0402	50V8C-D
HDMI IN OUT TXD0+	CV352	1	2	3.3P	0402	50V8C-D
HDMI IN OUT TXD1-	CV353	1	2	3.3P	0402	50V8C-D
HDMI IN OUT TXD1+	CV354	1	2	3.3P	0402	50V8C-D
HDMI IN OUT TXD2-	CV355	1	2	3.3P	0402	50V8C-D
HDMI IN OUT TXD2+	CV356	1	2	3.3P	0402	50V8C-D

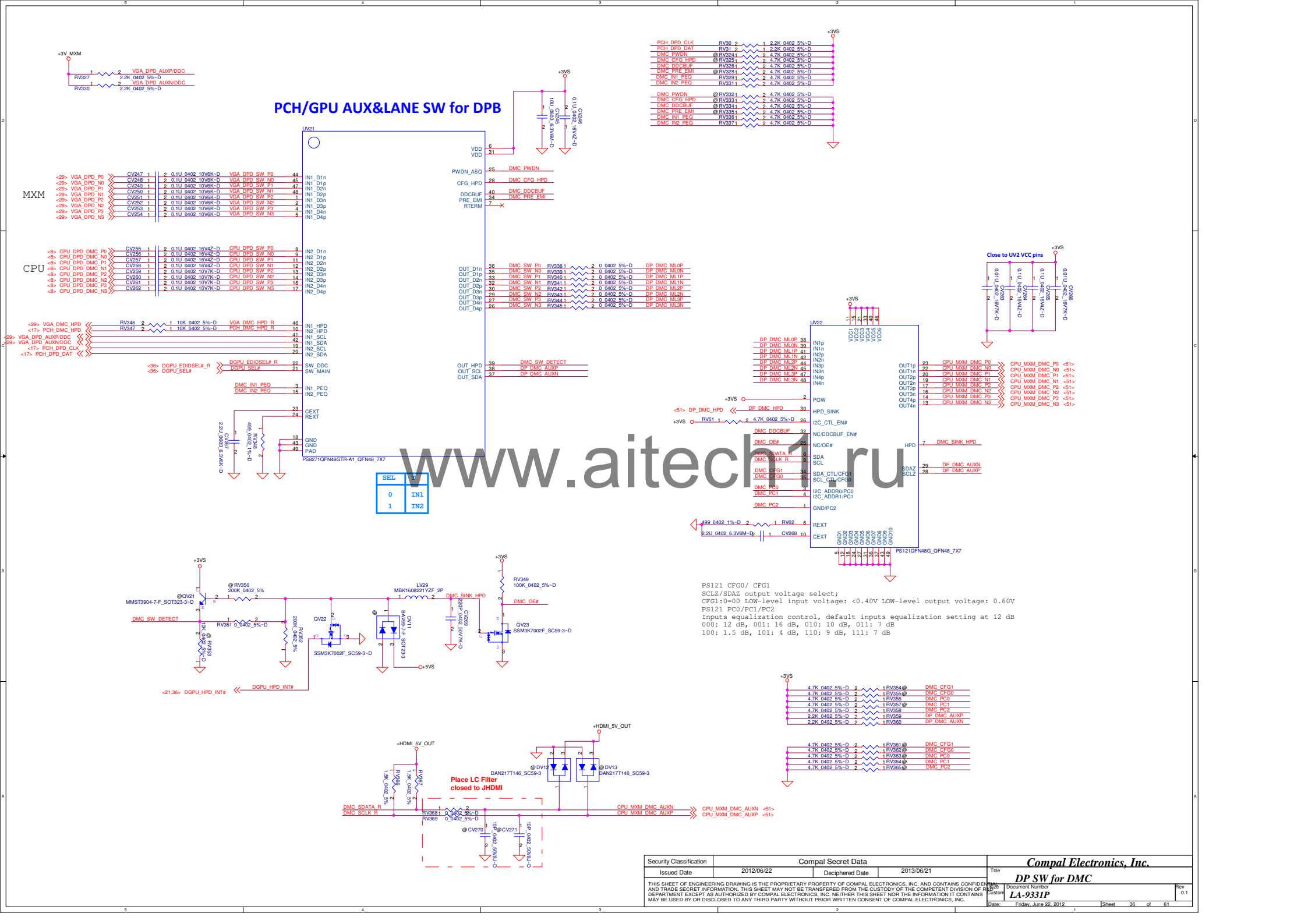
20120531 EMI ADD

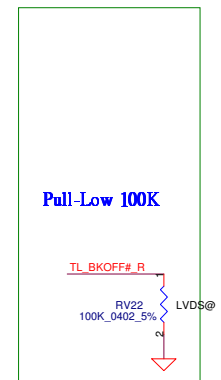
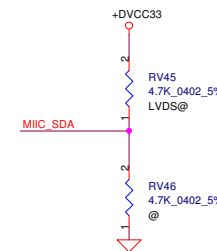
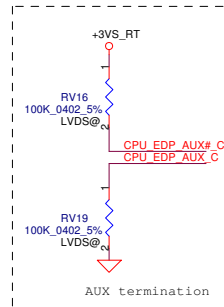
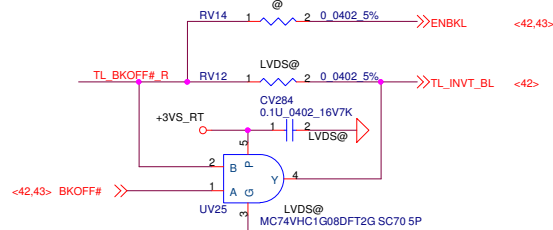
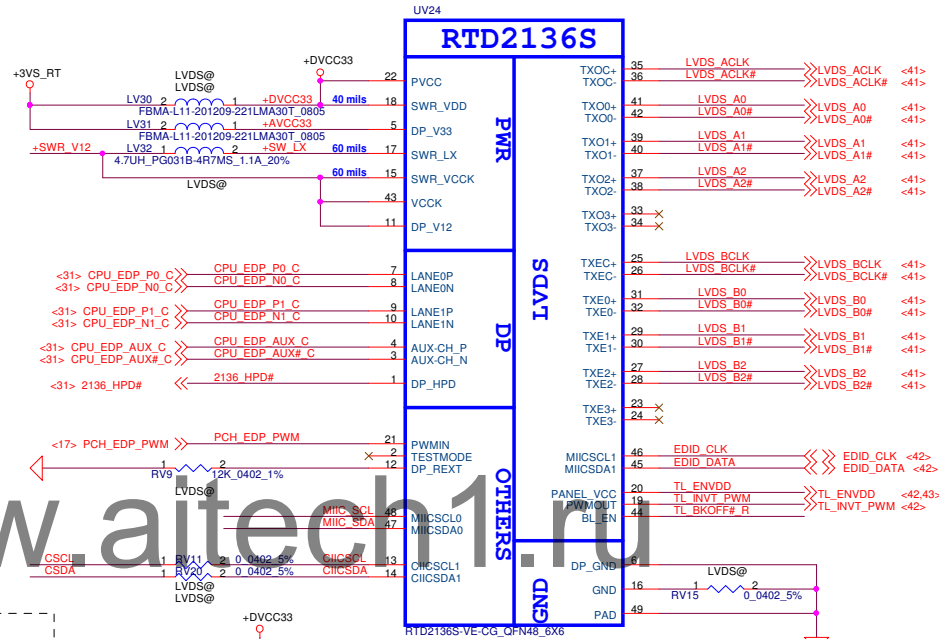
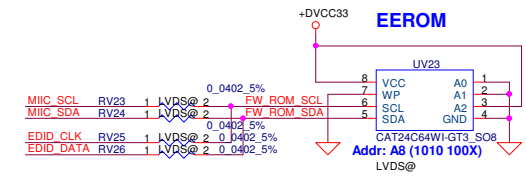
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2012/06/22	Deciphered Date	2013/06/21	Title	HDMI In/Out SW/Connector	
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				Customer		
				Date:	Friday, June 22, 2012	Sheet





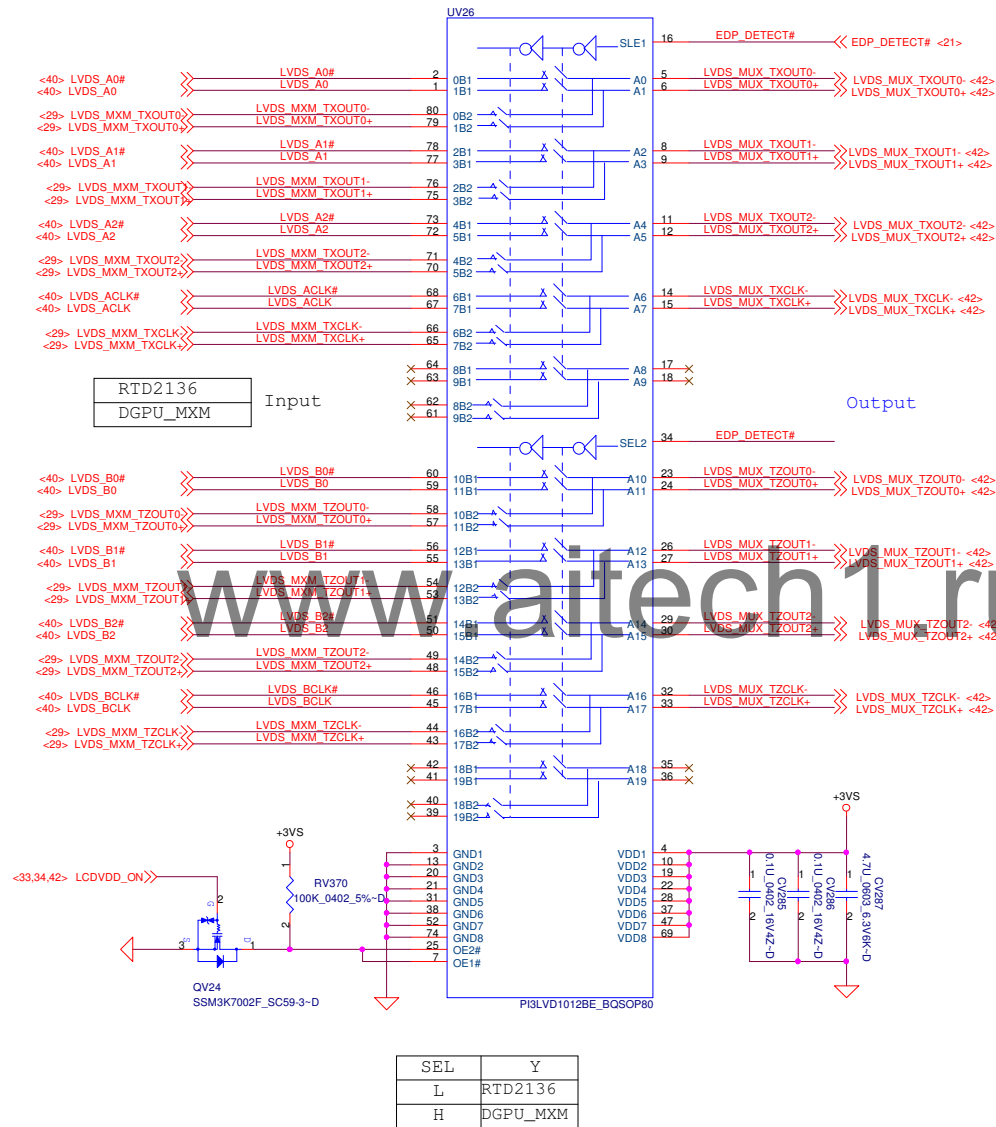






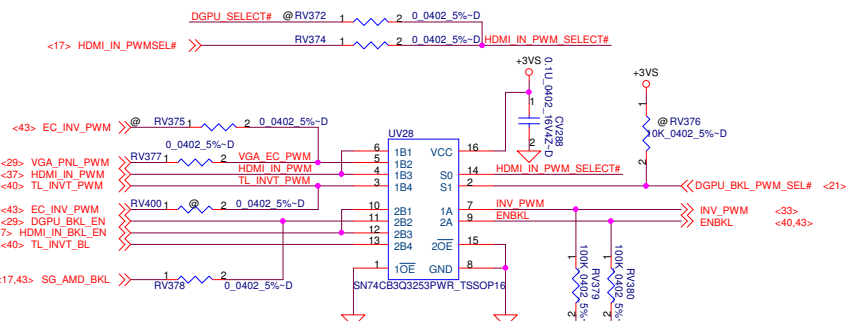
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STDP6038 SW STDP4028 PCH/GPU AUX for LVDS



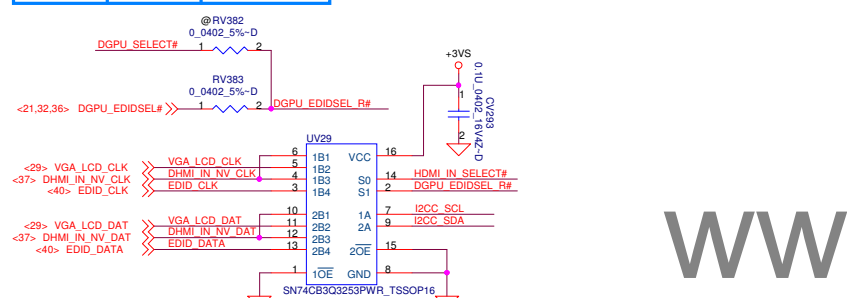
LCD Backlight Selector

PCH/GPU MUX & 6038 MUX SW for LVDS



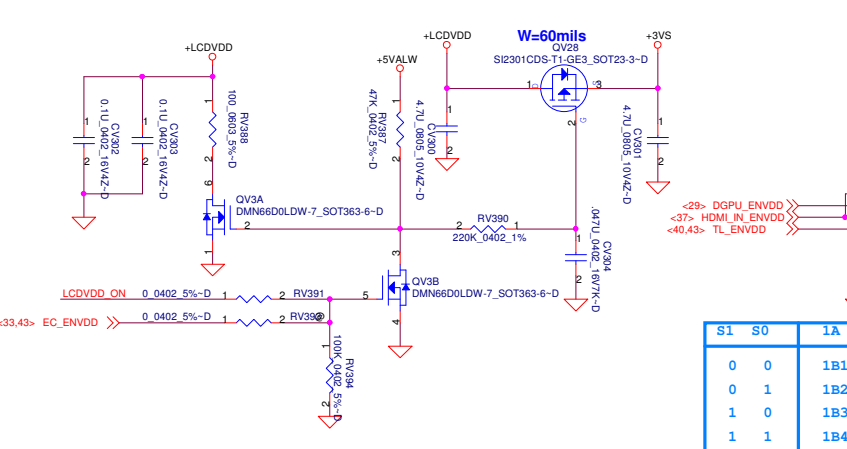
S1	S0	1A	2A	Y
0	0	1B1	2B1	HDMI IN (D)
0	1	1B2	2B2	DSC
1	0	1B3	2B3	HDMI IN (I)
1	1	1B4	2B4	UMA

LCD DDC Selector

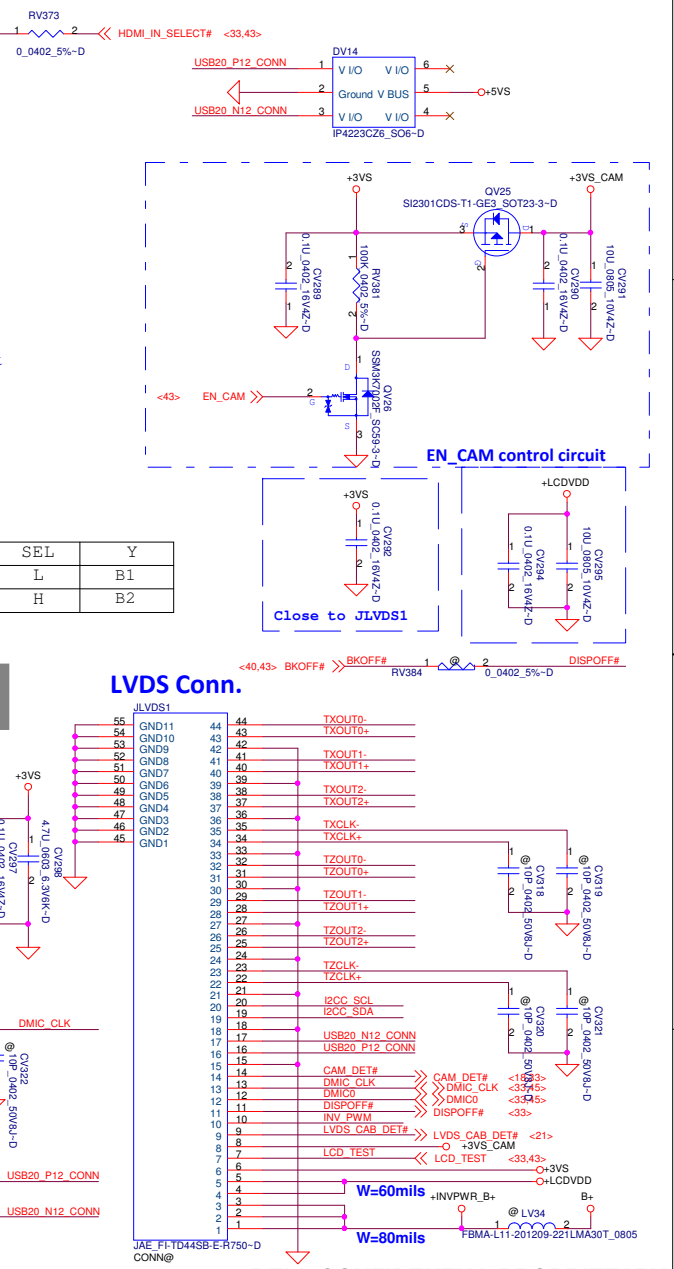
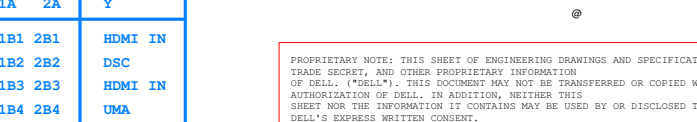
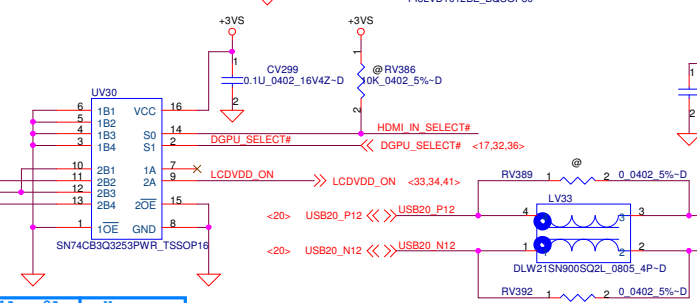
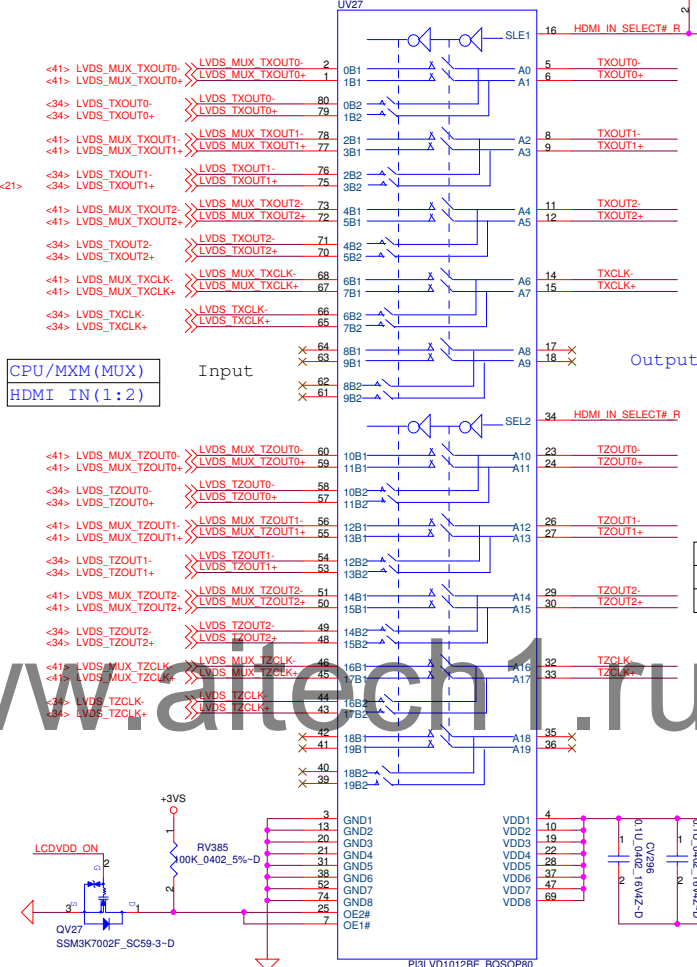


S1	S0	1A	2A	Y
0	0	1B1	2B1	HDMI IN (D)
0	1	1B2	2B2	DSC
1	0	1B3	2B3	HDMI IN (I)
1	1	1B4	2B4	UMA

LCD POWER



S1	S0	1A	2A	Y
0	0	1B1	2B1	HDMI IN
0	1	1B2	2B2	DSC
1	0	1B3	2B3	HDMI IN
1	1	1B4	2B4	UMA



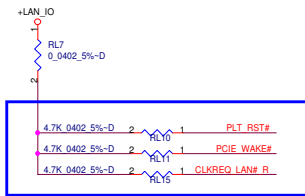
S1	S0	1A	2A	Y
0	0	1B1	2B1	HDMI IN
0	1	1B2	2B2	DSC
1	0	1B3	2B3	HDMI IN
1	1	1B4	2B4	UMA

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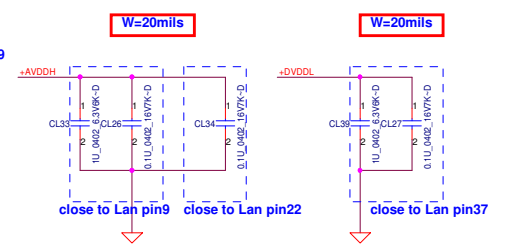
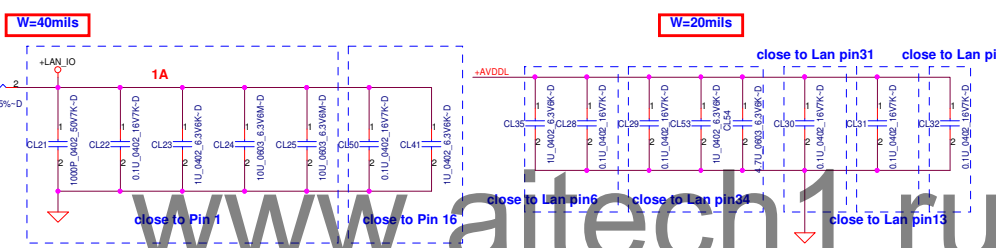
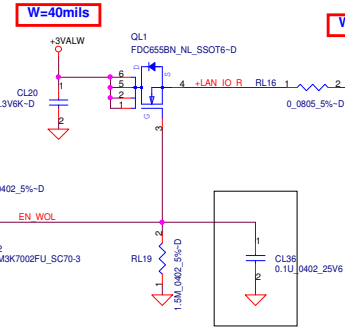
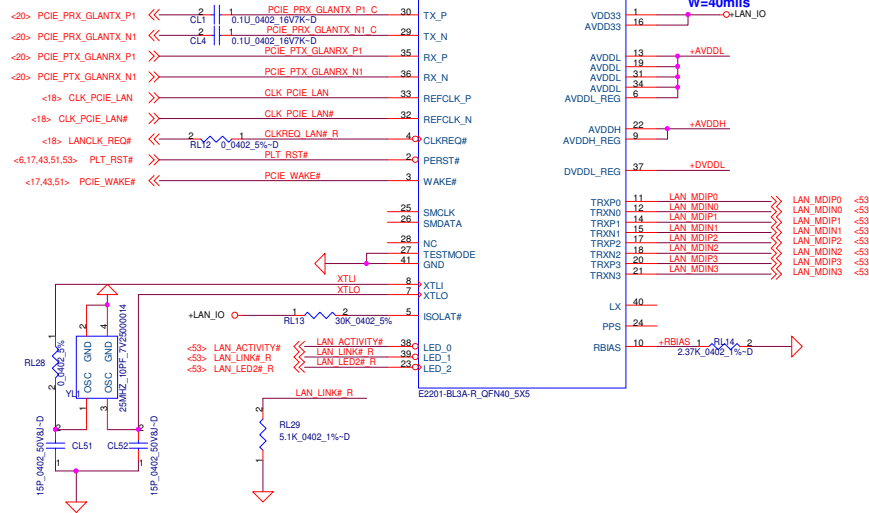


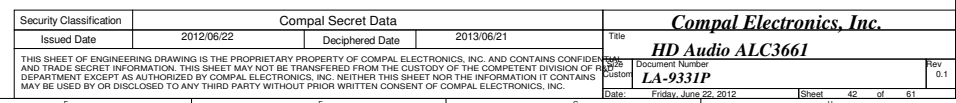
DELL CONFIDENTIAL/PROPRIETARY			
Compal Electronics, Inc.			
Title	Document Number	Rev	1
LVDS SW- 6038/SYSTEM & CONN	LA-9331P	0.1	
Date: Friday, June 22, 2012	Sheet 39 of 61		

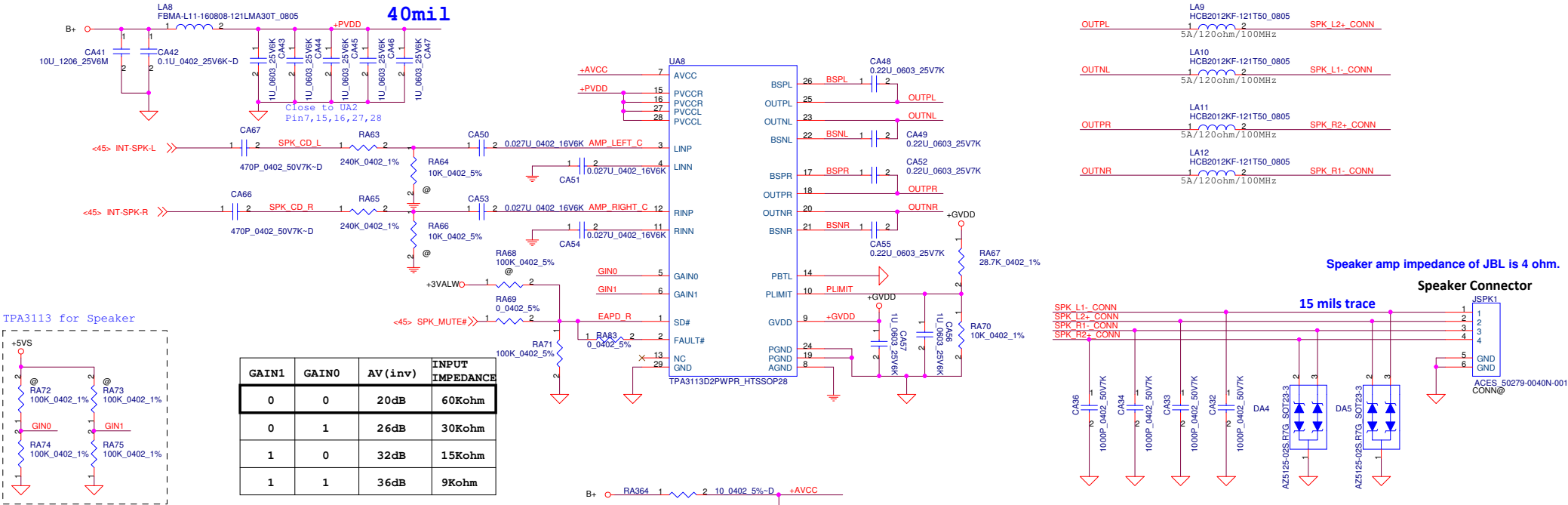
PCH_PWR_EN H_PROCHOT#_EC need add



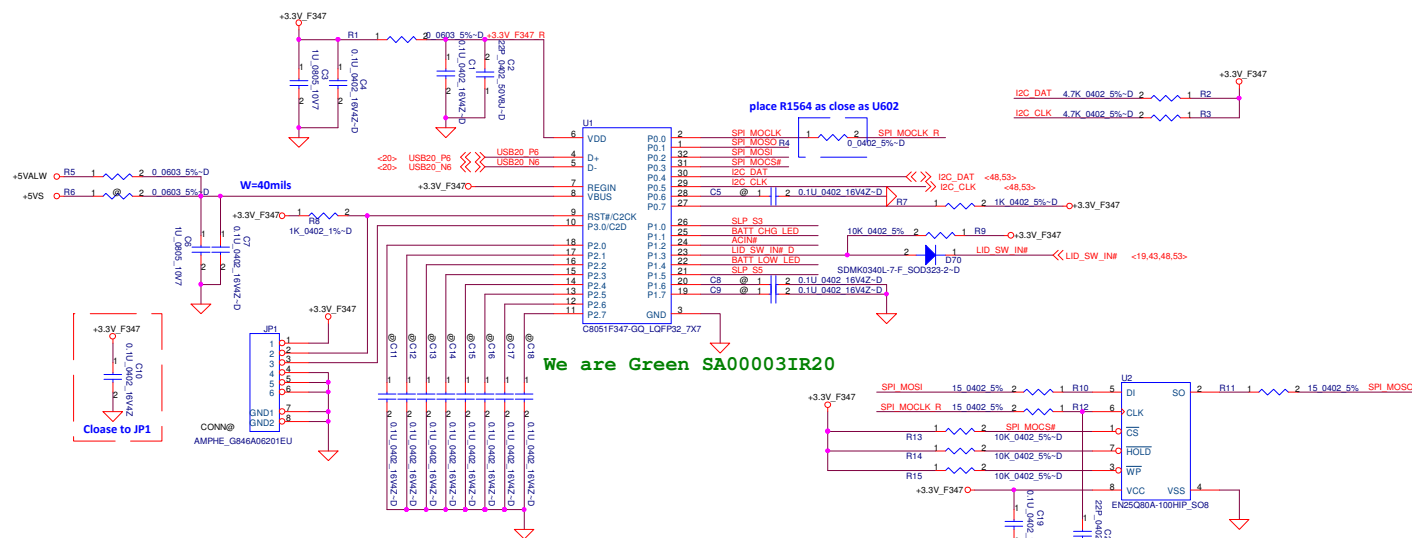
The pull-up resistors might not be necessary due to existence on PCH side.





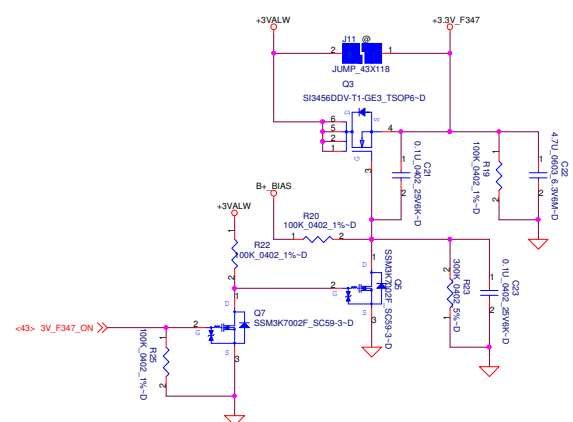
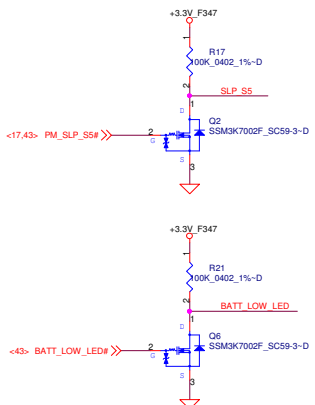
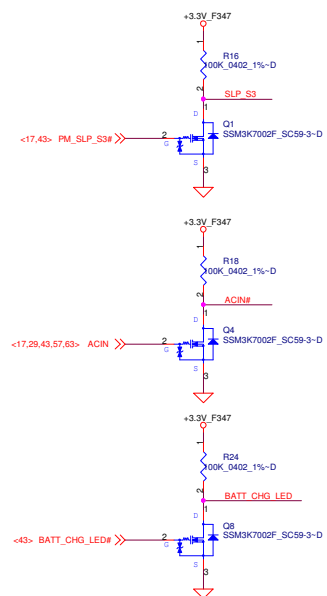


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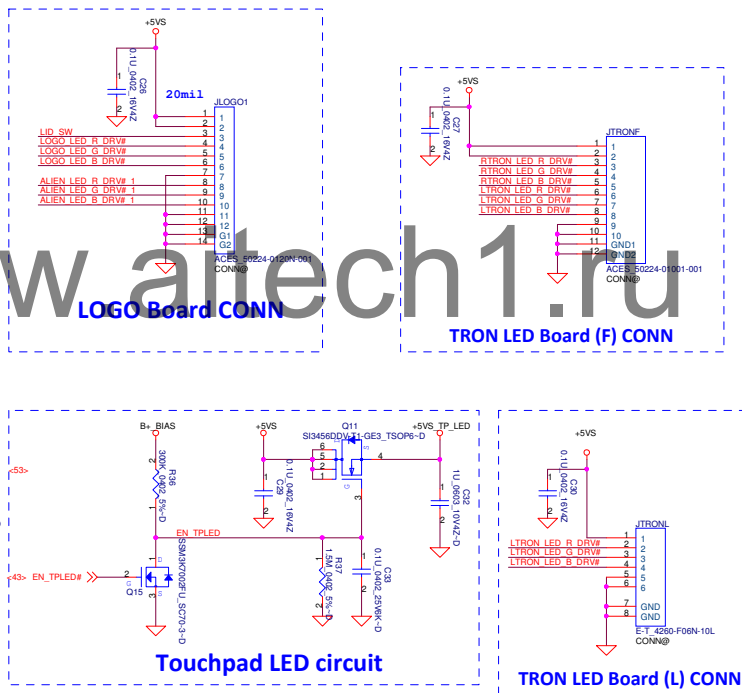
DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b



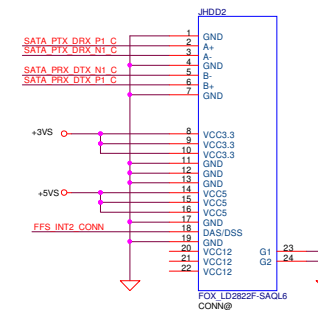
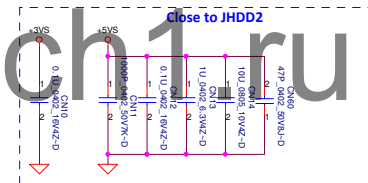
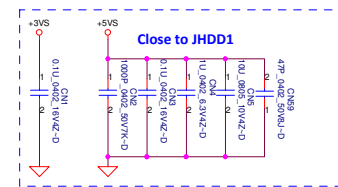
+3.3V_F347 behavior

	STATE				
	S0	S3	S4	S5	
AC IN	ON	ON	ON	ON	
BAT only	ON	ON	OFF	OFF	

AC mode battery full in S5=turn off ELC controller



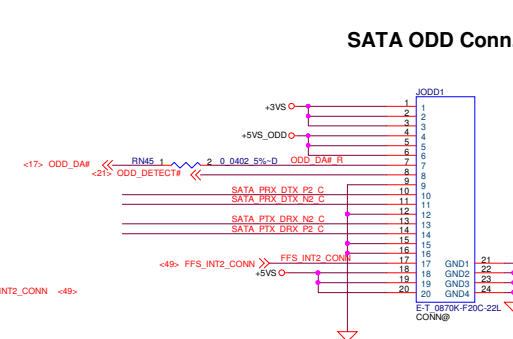
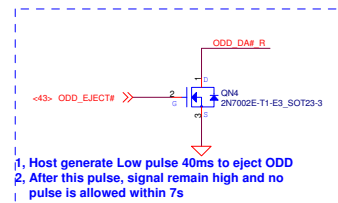
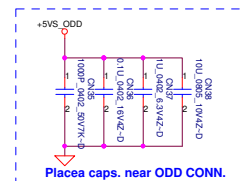
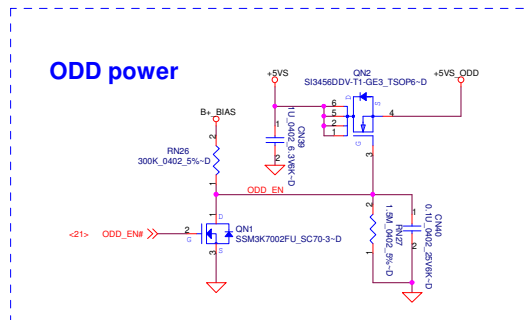
Reference	AD2	AD1	AD0	MAX7313
U605	0	1	0	Tron Lights,TP A-panel,B-Panel Logo
U608	0	1	1	Power Button, Media and Status LED Color
U?	1	0	0	Button, Indicator Brightness



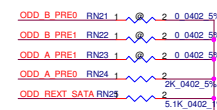
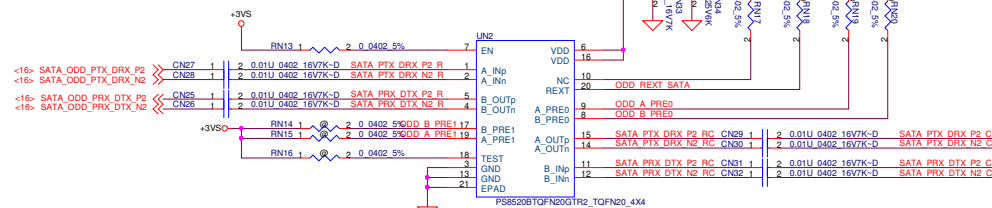
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Doc Number
LA-9331P

Rev
0.1



ODD Redriver

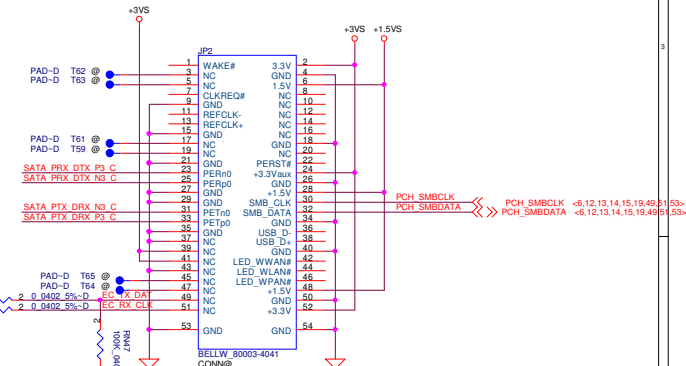
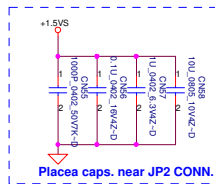
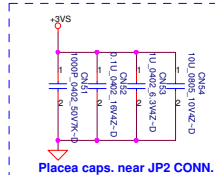
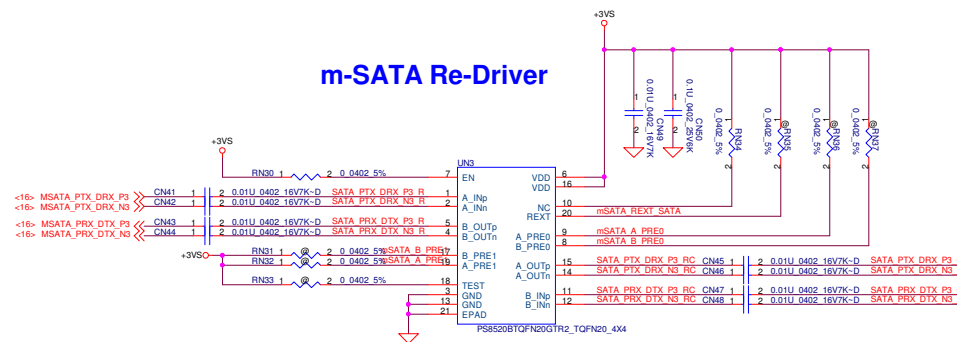


Pin 20:
PARADE PS8250B:
Reserve RN18, Mount RN25
PERICOM P13EQX6741ST:
Mount RN18, Reserve RN25
ASMEIDA ASM1466:
Mount RN18, Reserve RN25

Pin 9:
PARADE PS8250B:
Reserve RN24
PERICOM P13EQX6741ST:
Reserve RN24
ASMEIDA ASM1466:
Mount RN24 to pull down

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m-SATA Re-Driver

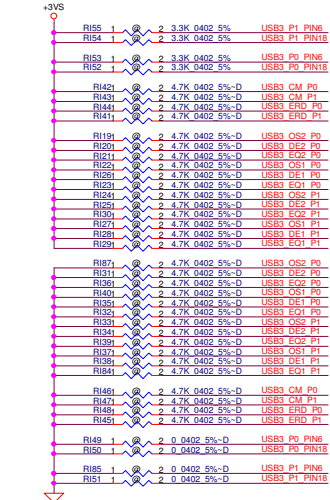
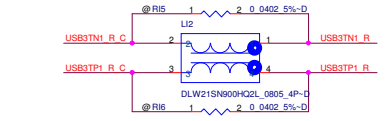
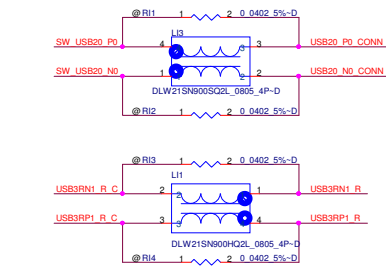


Pin 20:
PARADE PS8250B:
Reserve RN35, Mount RN42
PERICOM P13EQX6741ST:
Mount RN35, Reserve RN42
ASMEIDA ASM1466:
Mount RN35, Reserve RN42

Pin 9:
PARADE PS8250B:
Reserve RN41
PERICOM P13EQX6741ST:
Reserve RN41
ASMEIDA ASM1466:
Mount RN41 to pull down

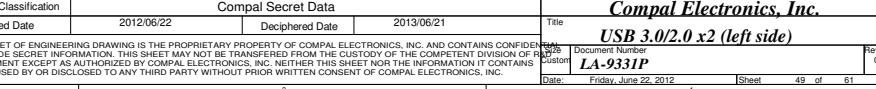
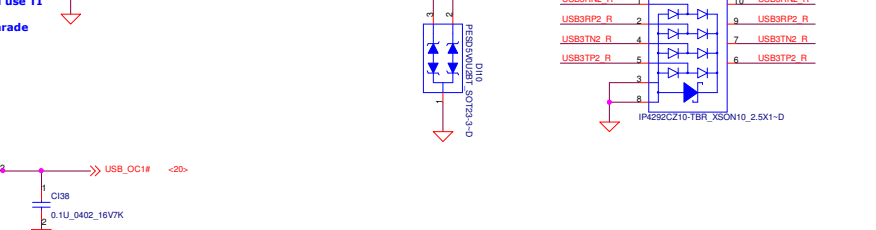
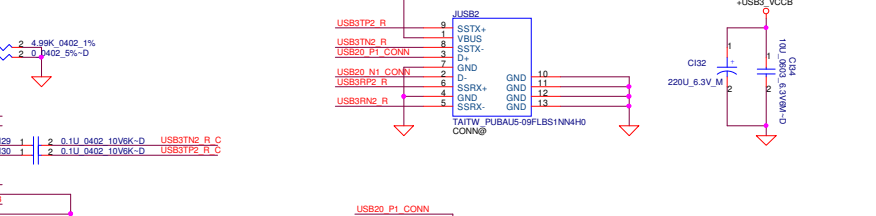
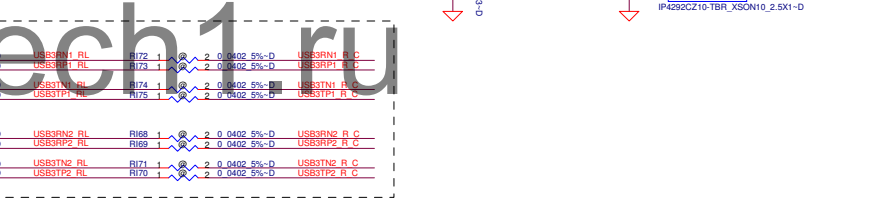
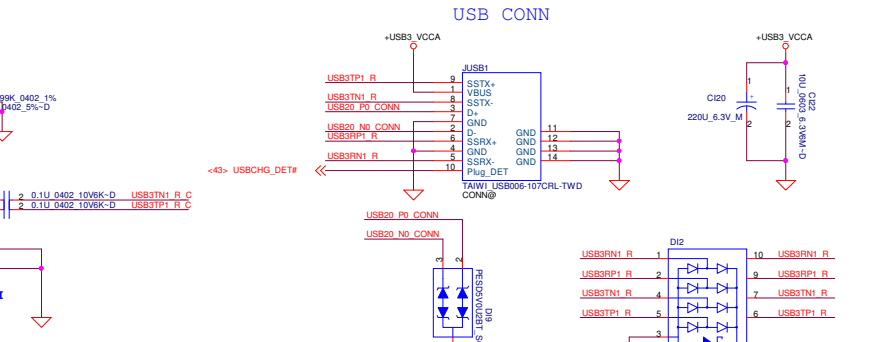
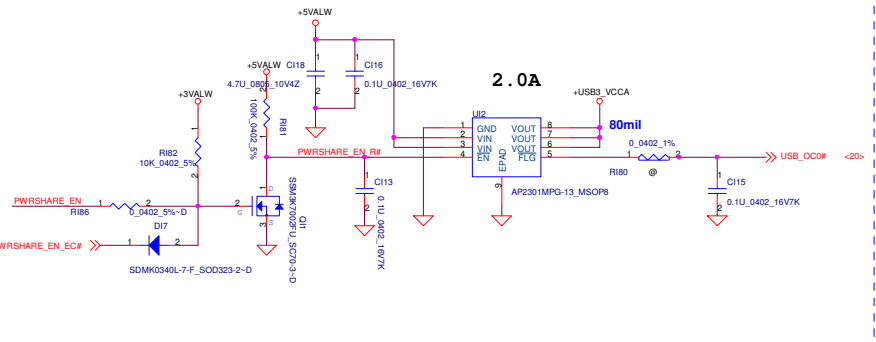
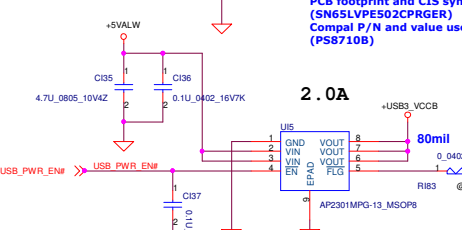
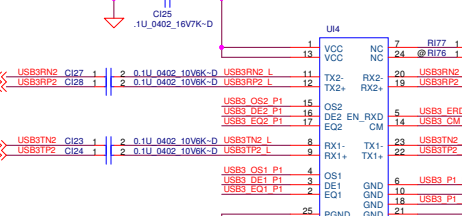
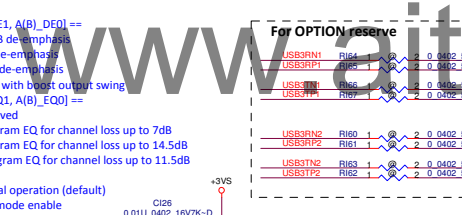
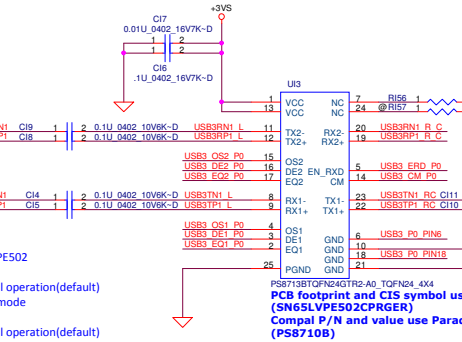
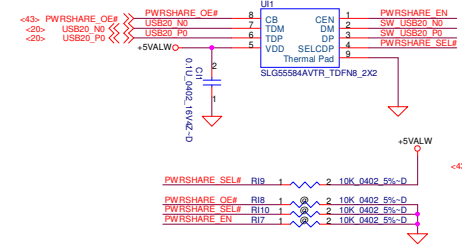
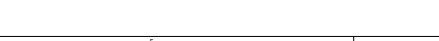
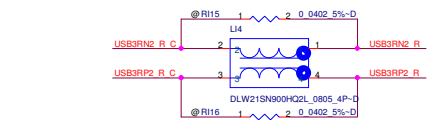
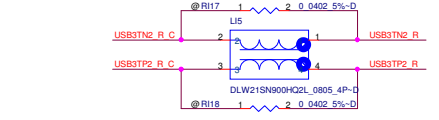
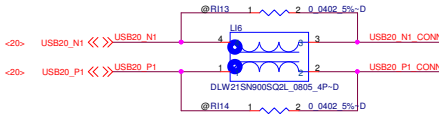
mSATA B_P00 RN38 1 2 0.0402 5%
mSATA B_P01 RN39 1 2 0.0402 5%
mSATA A_P01 RN40 1 2 0.0402 5%
mSATA A_P00 RN41 1 2 0.0402 5%
mSATA REXT_SATA RN42 2 2K_0402 5%
5.1K_0402 1%

Power share

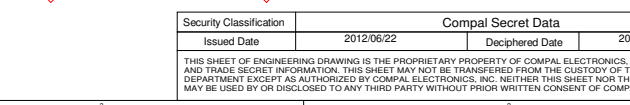
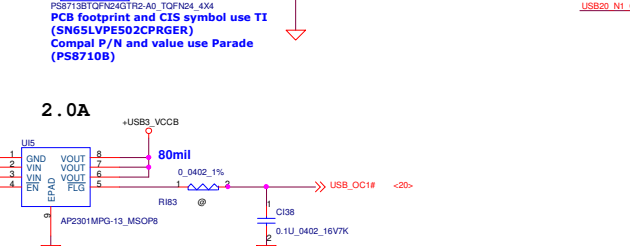
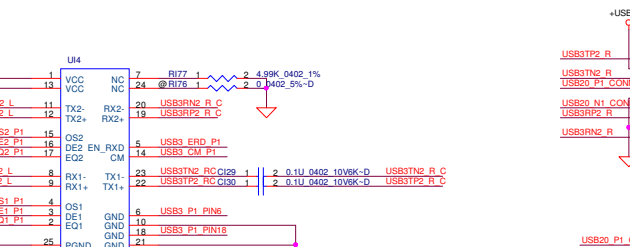
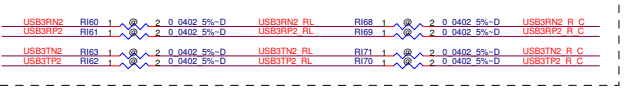


Vendor pin	PS8710B (default)	TI
pin15	AEQ1	OS2
pin16	ADE0	DE2
pin17	AEQ0	EQ2
pin4	BEQ1	OS1
pin3	BDE0	DE1
pin2	BEQ0	EQ1
pin5	PD	EN_RXD
pin14	TEST	CM
pin18	ADE1	
pin6	BDE1	

[Parade suggest]
PS8710 AEQ0, BEQ0 adjust 7db,
REXT use 3.3 K well get better test result.



For OPTION reserve
[A(B)_DE1, A(B)_DE0] ==
LL: 3.5db de-emphasis
LH: No de-emphasis
HL: 7db de-emphasis
HH: 5db with boost output swing
[A(B)_EQ1, A(B)_EQ0] ==
LL: reserved
LH: program EQ for channel loss up to 7db
HL: program EQ for channel loss up to 14.5db
HH: program EQ for channel loss up to 11.5db
TEST ==
L: Normal operation (default)
H: Test mode enable



Security Classification	Compal Secret Data				Title	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	USB 3.0/2.0 x2 (left side)		
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				Date	LA-931P	
				Date	Friday, June 22, 2012	
				Sheet	49	of 61

BTB CONNECTOR TO USB3.0 Board

50-pin connector (J101) pinout:

- Pin 1: +5VSW
- Pin 2: +5VALW
- Pin 3: +5VSW
- Pin 4: USB20_N2
- Pin 5: USB20_P2
- Pin 6: USB3TP5
- Pin 7: USB3TN5
- Pin 8: USB3RP5
- Pin 9: USB3RN5
- Pin 10: USB20_N3
- Pin 11: USB20_P3
- Pin 12: USB3TP6
- Pin 13: USB3TN6
- Pin 14: USB3RP6
- Pin 15: USB3RN6
- Pin 16: USB_OC2#
- Pin 17: USB_OC3#
- Pin 18: USB3TP5
- Pin 19: USB3TN5
- Pin 20: USB3RP5
- Pin 21: USB3RN5
- Pin 22: USB20_N3
- Pin 23: USB20_P3
- Pin 24: USB3TP6
- Pin 25: USB3TN6
- Pin 26: USB3RP6
- Pin 27: USB3RN6
- Pin 28: USB_OC2#
- Pin 29: USB_OC3#
- Pin 30: USB3TP5
- Pin 31: USB3TN5
- Pin 32: USB3RP5
- Pin 33: USB3RN5
- Pin 34: USB20_N3
- Pin 35: USB20_P3
- Pin 36: USB3TP6
- Pin 37: USB3TN6
- Pin 38: USB3RP6
- Pin 39: USB3RN6
- Pin 40: USB_OC2#
- Pin 41: USB_OC3#
- Pin 42: USB3TP5
- Pin 43: USB3TN5
- Pin 44: USB3RP5
- Pin 45: USB3RN5
- Pin 46: USB20_N3
- Pin 47: USB20_P3
- Pin 48: USB3TP6
- Pin 49: USB3TN6
- Pin 50: USB3RP6

USB3.0 connector (J102) pinout:

- Pin 1: +5VSW
- Pin 2: +5VALW
- Pin 3: +5VSW
- Pin 4: USB3TP5
- Pin 5: USB3TN5
- Pin 6: USB3RP5
- Pin 7: USB3RN5
- Pin 8: USB20_N3
- Pin 9: USB20_P3
- Pin 10: USB3TP6
- Pin 11: USB3TN6
- Pin 12: USB3RP6
- Pin 13: USB3RN6
- Pin 14: USB_OC2#
- Pin 15: USB_OC3#
- Pin 16: USB3TP5
- Pin 17: USB3TN5
- Pin 18: USB3RP5
- Pin 19: USB3RN5
- Pin 20: USB20_N3
- Pin 21: USB20_P3
- Pin 22: USB3TP6
- Pin 23: USB3TN6
- Pin 24: USB3RP6
- Pin 25: USB3RN6
- Pin 26: USB_OC2#
- Pin 27: USB_OC3#
- Pin 28: USB3TP5
- Pin 29: USB3TN5
- Pin 30: USB3RP5
- Pin 31: USB3RN5
- Pin 32: USB20_N3
- Pin 33: USB20_P3
- Pin 34: USB3TP6
- Pin 35: USB3TN6
- Pin 36: USB3RP6
- Pin 37: USB3RN6
- Pin 38: USB_OC2#
- Pin 39: USB_OC3#
- Pin 40: USB3TP5
- Pin 41: USB3TN5
- Pin 42: USB3RP5
- Pin 43: USB3RN5
- Pin 44: USB20_N3
- Pin 45: USB20_P3
- Pin 46: USB3TP6
- Pin 47: USB3TN6
- Pin 48: USB3RP6
- Pin 49: USB3RN6
- Pin 50: USB_OC2#

USB3.0 connector (J102) pinout (continued):

- Pin 51: GND1
- Pin 52: GND2
- Pin 53: E&T_1001-F50E-03R
- Pin 54: CONN@

USB3.0 connector (J102) pinout (continued):

- Pin 55: +5VSW
- Pin 56: +5VALW
- Pin 57: +5VSW
- Pin 58: USB3TP5
- Pin 59: USB3TN5
- Pin 60: USB3RP5
- Pin 61: USB3RN5
- Pin 62: USB20_N3
- Pin 63: USB20_P3
- Pin 64: USB3TP6
- Pin 65: USB3TN6
- Pin 66: USB3RP6
- Pin 67: USB3RN6
- Pin 68: USB_OC2#
- Pin 69: USB_OC3#
- Pin 70: USB3TP5
- Pin 71: USB3TN5
- Pin 72: USB3RP5
- Pin 73: USB3RN5
- Pin 74: USB20_N3
- Pin 75: USB20_P3
- Pin 76: USB3TP6
- Pin 77: USB3TN6
- Pin 78: USB3RP6
- Pin 79: USB3RN6
- Pin 80: USB_OC2#
- Pin 81: USB_OC3#
- Pin 82: USB3TP5
- Pin 83: USB3TN5
- Pin 84: USB3RP5
- Pin 85: USB3RN5
- Pin 86: USB20_N3
- Pin 87: USB20_P3
- Pin 88: USB3TP6
- Pin 89: USB3TN6
- Pin 90: USB3RP6
- Pin 91: USB3RN6
- Pin 92: USB_OC2#
- Pin 93: USB_OC3#
- Pin 94: USB3TP5
- Pin 95: USB3TN5
- Pin 96: USB3RP5
- Pin 97: USB3RN5
- Pin 98: USB20_N3
- Pin 99: USB20_P3
- Pin 100: USB3TP6

USB3.0 connector (J102) pinout (continued):

- Pin 101: USB3TN6
- Pin 102: USB3RP6
- Pin 103: USB3RN6
- Pin 104: USB_OC2#
- Pin 105: USB_OC3#
- Pin 106: USB3TP5
- Pin 107: USB3TN5
- Pin 108: USB3RP5
- Pin 109: USB3RN5
- Pin 110: USB20_N3
- Pin 111: USB20_P3
- Pin 112: USB3TP6
- Pin 113: USB3TN6
- Pin 114: USB3RP6
- Pin 115: USB3RN6
- Pin 116: USB_OC2#
- Pin 117: USB_OC3#
- Pin 118: USB3TP5
- Pin 119: USB3TN5
- Pin 120: USB3RP5
- Pin 121: USB3RN5
- Pin 122: USB20_N3
- Pin 123: USB20_P3
- Pin 124: USB3TP6
- Pin 125: USB3TN6
- Pin 126: USB3RP6
- Pin 127: USB3RN6
- Pin 128: USB_OC2#
- Pin 129: USB_OC3#
- Pin 130: USB3TP5
- Pin 131: USB3TN5
- Pin 132: USB3RP5
- Pin 133: USB3RN5
- Pin 134: USB20_N3
- Pin 135: USB20_P3
- Pin 136: USB3TP6
- Pin 137: USB3TN6
- Pin 138: USB3RP6
- Pin 139: USB3RN6
- Pin 140: USB_OC2#
- Pin 141: USB_OC3#
- Pin 142: USB3TP5
- Pin 143: USB3TN5
- Pin 144: USB3RP5
- Pin 145: USB3RN5
- Pin 146: USB20_N3
- Pin 147: USB20_P3
- Pin 148: USB3TP6
- Pin 149: USB3TN6
- Pin 150: USB3RP6

USB3.0 connector (J102) pinout (continued):

- Pin 151: USB3TN6
- Pin 152: USB3RP6
- Pin 153: USB3RN6
- Pin 154: USB_OC2#
- Pin 155: USB_OC3#
- Pin 156: USB3TP5
- Pin 157: USB3TN5
- Pin 158: USB3RP5
- Pin 159: USB3RN5
- Pin 160: USB20_N3
- Pin 161: USB20_P3
- Pin 162: USB3TP6
- Pin 163: USB3TN6
- Pin 164: USB3RP6
- Pin 165: USB3RN6
- Pin 166: USB_OC2#
- Pin 167: USB_OC3#
- Pin 168: USB3TP5
- Pin 169: USB3TN5
- Pin 170: USB3RP5
- Pin 171: USB3RN5
- Pin 172: USB20_N3
- Pin 173: USB20_P3
- Pin 174: USB3TP6
- Pin 175: USB3TN6
- Pin 176: USB3RP6
- Pin 177: USB3RN6
- Pin 178: USB_OC2#
- Pin 179: USB_OC3#
- Pin 180: USB3TP5
- Pin 181: USB3TN5
- Pin 182: USB3RP5
- Pin 183: USB3RN5
- Pin 184: USB20_N3
- Pin 185: USB20_P3
- Pin 186: USB3TP6
- Pin 187

Pinout diagram for the CV1LU CP25602D0R0-Q5-NH connector. The diagram shows a 60-pin connector with pins numbered 1 to 60. Pins 1-19 are on the left, and pins 20-60 are on the right. The diagram includes various signal names and their corresponding pin numbers. A note indicates that pins 16 and 17 are reserved for a key pad (Viking only). A large watermark 'n1.ru' is visible across the bottom left of the diagram.

Signal	Pin
+5VS_TP_LED#	1
	2
	3
<43> TP_CLK	4
<43> TP_DATA	5
	6
	7
<6,12,13,14,15,19,49,50,51> PCH_SMBDATA	8
<6,12,13,14,15,19,49,50,51> PCH_SMBCLK	9
<48> TP_LED_R_DRV#	10
<48> TP_LED_G_DRV#	11
<48> TP_LED_B_DRV#	12
	13
	14
<43> VPK_DET#	15
<43> VPK_EN	16
Reserve for Key Pad (Viking only)	17
	18
	19
+5VS	20
	21
+3VS	22
<19,40,43,54> EC_SMB_DA2	23
<19,40,43,54> EC_SMB_CK2	24
	25
<20> USB20_P13	26
<20> USB20_N13	27
	28
<47,48> I2C_CLK	29
<47,48> I2C_DAT	30
<48> 7313_INT#	31
+3.3V_F347C	32
<43> KB_DET#	33
	34
KS10	35
KS11	36
KS12	37
KS13	38
KS14	39
KS15	40
KS16	41
KS17	42
KS20	43
KSO1	44
KSO2	45
KSO3	46
KSO4	47
KSO5	48
KSO6	49
KSO7	50
KSO8	51
KSO9	52
KSO10	53
KSO11	54
KSO12	55
KSO13	56
KSO14	57
KSO15	58
KSO16	59
KSO17	60

Additional signals and pins shown in the diagram:

- Pin 16: Reserve for Key Pad (Viking only)
- Pin 17: Reserve for Key Pad (Viking only)
- Pin 18: Reserve for Key Pad (Viking only)
- Pin 19: Reserve for Key Pad (Viking only)
- Pin 20: +5VS
- Pin 21: +3VS
- Pin 22: <19,40,43,54> EC_SMB_DA2
- Pin 23: <19,40,43,54> EC_SMB_CK2
- Pin 24: <20> USB20_P13
- Pin 25: <20> USB20_N13
- Pin 26: <47,48> I2C_CLK
- Pin 27: <47,48> I2C_DAT
- Pin 28: <48> 7313_INT#
- Pin 29: +3.3V_F347C
- Pin 30: <43> KB_DET#
- Pin 31: KS10
- Pin 32: KS11
- Pin 33: KS12
- Pin 34: KS13
- Pin 35: KS14
- Pin 36: KS15
- Pin 37: KS16
- Pin 38: KS17
- Pin 39: KS20
- Pin 40: KSO1
- Pin 41: KSO2
- Pin 42: KSO3
- Pin 43: KSO4
- Pin 44: KSO5
- Pin 45: KSO6
- Pin 46: KSO7
- Pin 47: KSO8
- Pin 48: KSO9
- Pin 49: KSO10
- Pin 50: KSO11
- Pin 51: KSO12
- Pin 52: KSO13
- Pin 53: KSO14
- Pin 54: KSO15
- Pin 55: KSO16
- Pin 56: KSO17

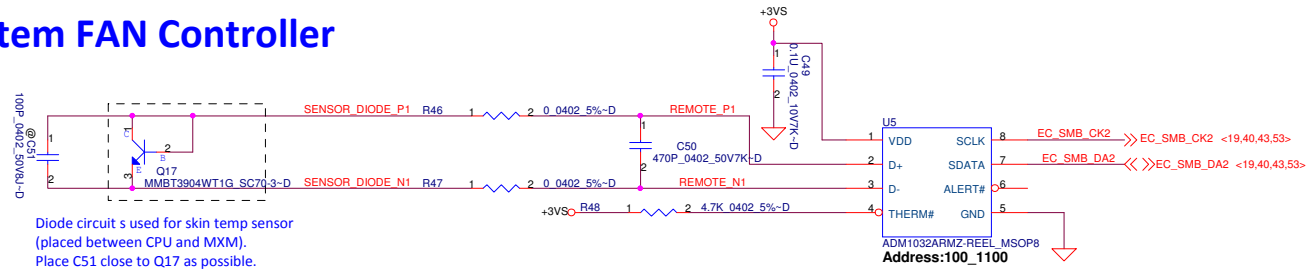
Place close to J102

Pin	Signal
1	<20> PCIE_PT_X_CARDRX_P4
2	PCIE_PT_X_CARDRX_P4
3	<20> PCIE_PT_X_CARDRX_N4
4	PCIE_PT_X_CARDRX_N4
5	<20> PCIE_PR_X_CARDTX_P4
6	PCIE_PR_X_CARDTX_P4
7	<20> PCIE_PR_X_CARDTX_N4
8	PCIE_PR_X_CARDTX_N4
9	<18> CLK_PCIE_CD
10	CLK_PCIE_CD
11	<18> CLK_PCIE_CD#
12	CLK_PCIE_CD#
13	<6,17,43,44,51> PLT_RST#
14	PLT_RST#
15	<18> CDCLK_REQ#
16	CDCLK_REQ#
17	+3VSW
18	+5VSW
19	+3VSW
20	+5VSW
21	<48> LED_R_7313#_1
22	LED_R_7313#_1
23	<48> LED_B_7313#_1
24	LED_B_7313#_1
25	<48> LED_G_7313#_1
26	LED_G_7313#_1
27	<43> CAPS_LED#
28	WLES_ON/OFF_LED#
29	<48> HDD_R
30	HDD_R
31	<48> HDD_G
32	HDD_G
G1	<48> HDD_B
G2	HDD_B
	<55> ON/OFFBTN#
	LID_SW
	<19,43,47,48> LID_SW_IN#
	LID_SW_IN#
	<48> PWR_R_7313#
	PWR_R_7313#
	<48> PWR_B_7313#
	PWR_B_7313#

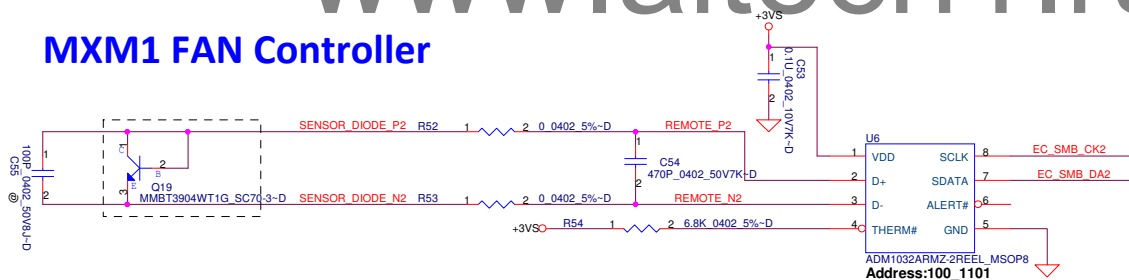
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CONN@

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				Rev 0.1	
				Date: Friday, June 22, 2012 Sheet 50 of 61	

System FAN Controller



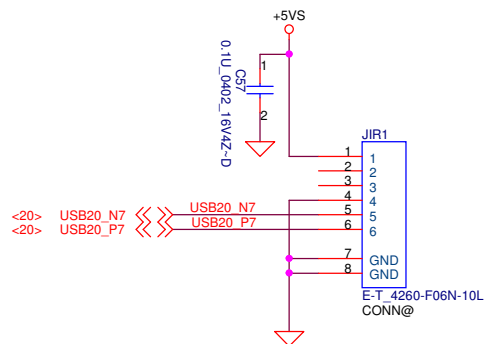
MXM1 FAN Controller



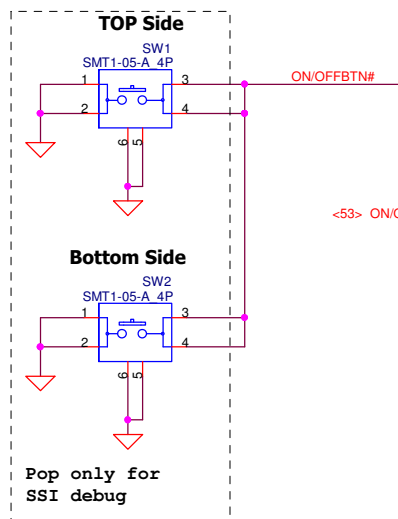
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				Date:	Friday, June 22, 2012
				Sheet	51 of 61
				Rev	0.1

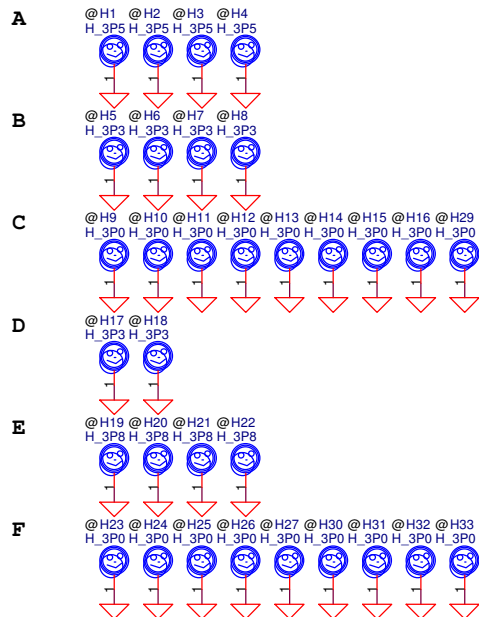
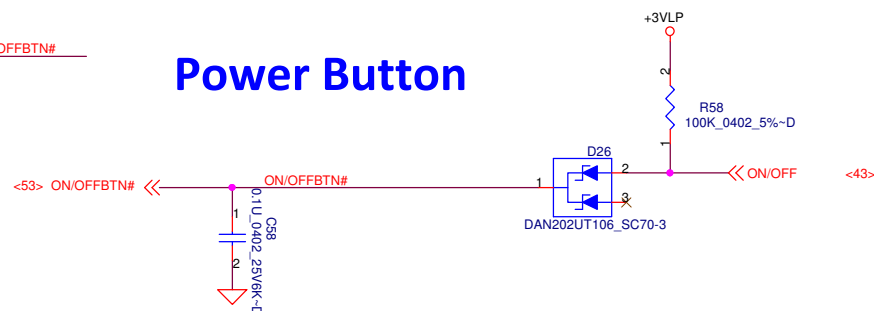
IR SENSOR connector



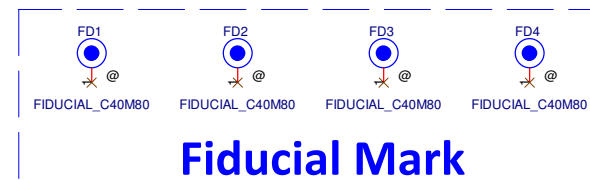
ON/OFF switch



Power Button

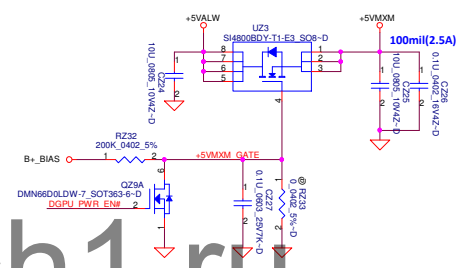
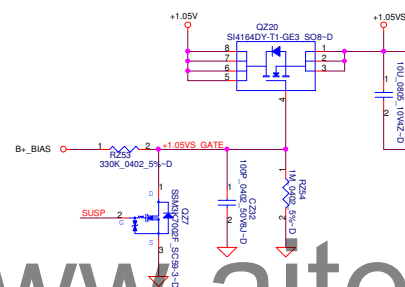
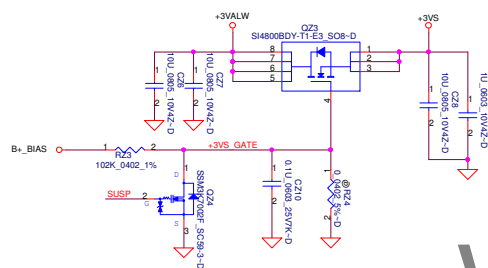
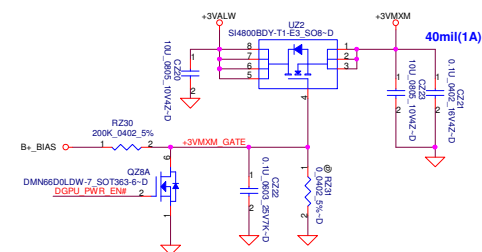
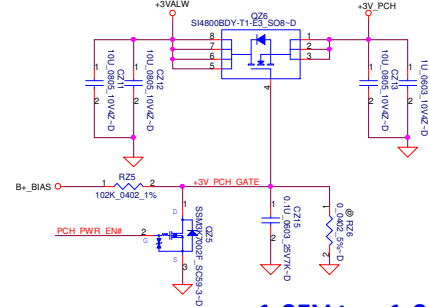
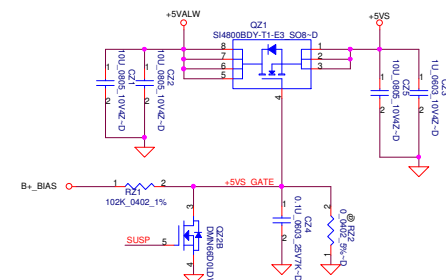


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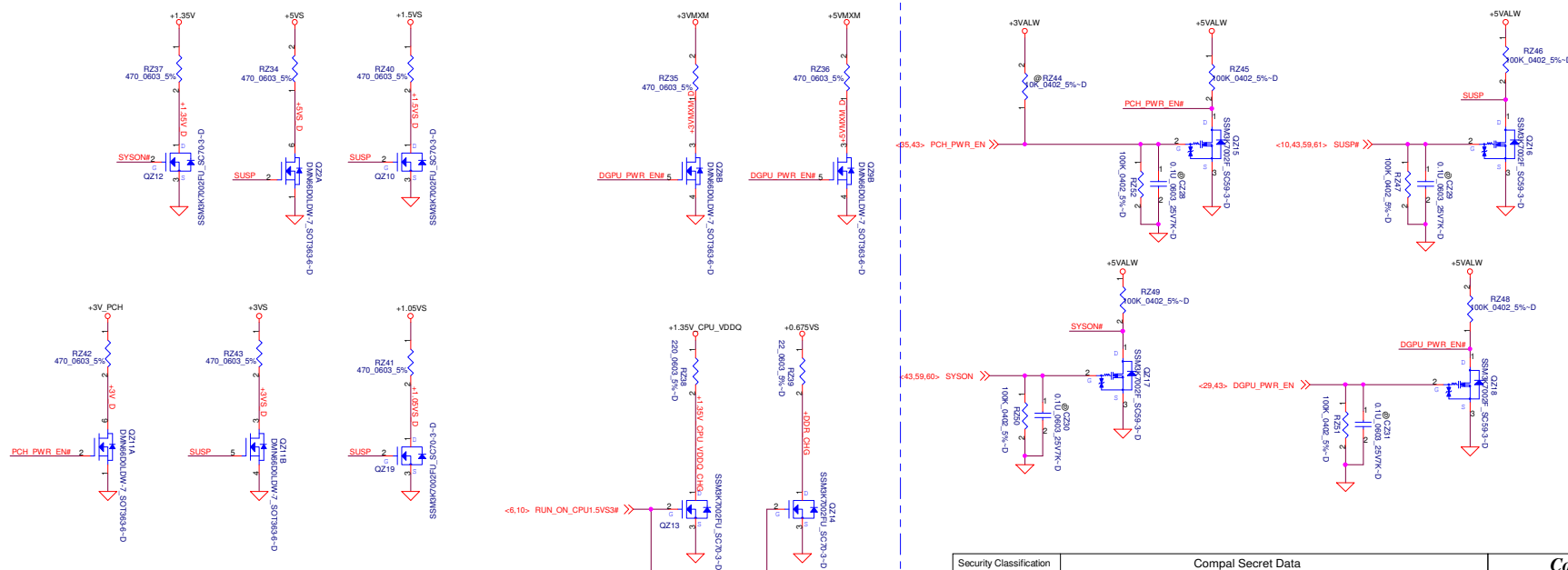


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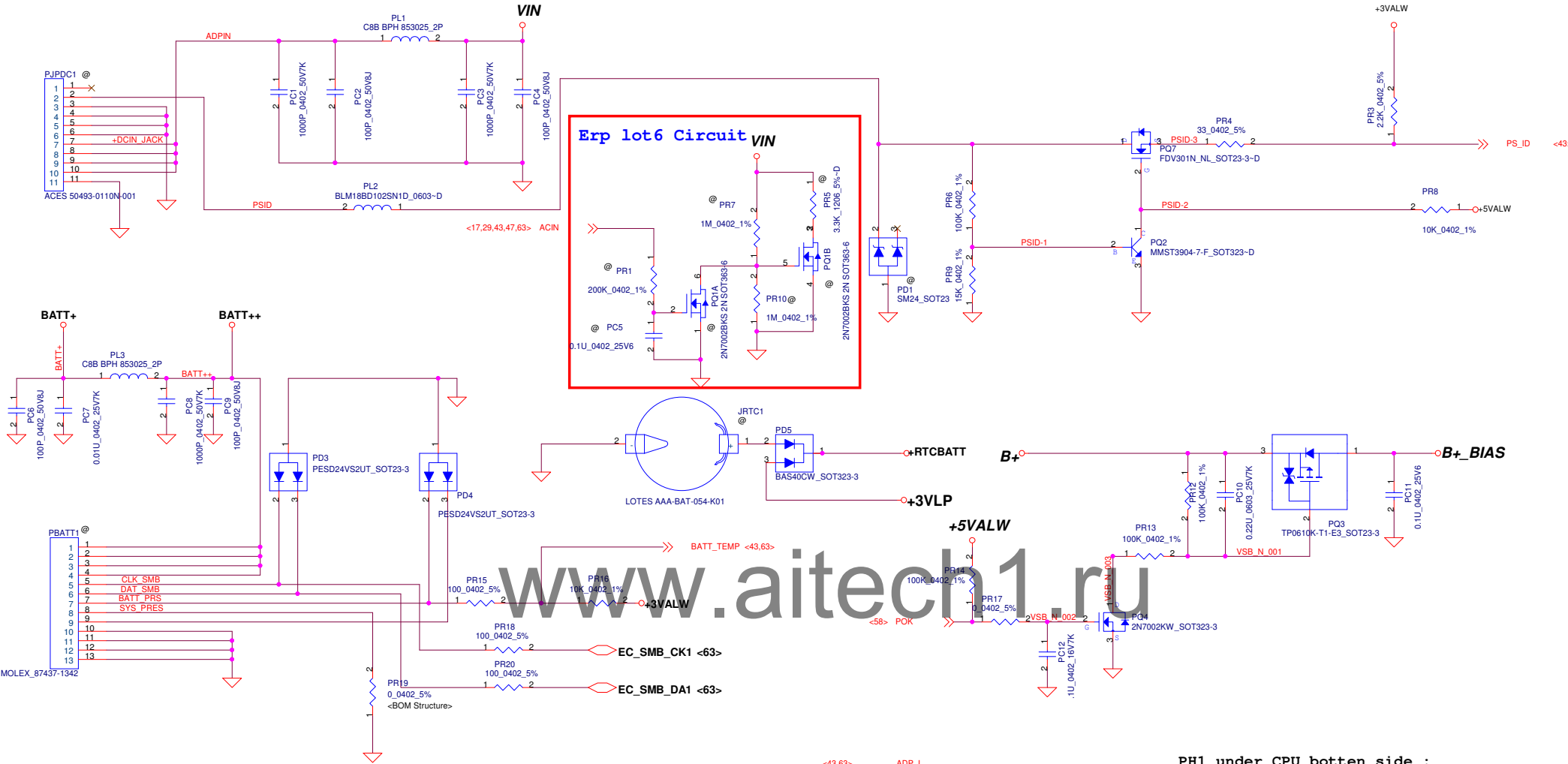
DC to DC



Discharge Circuit

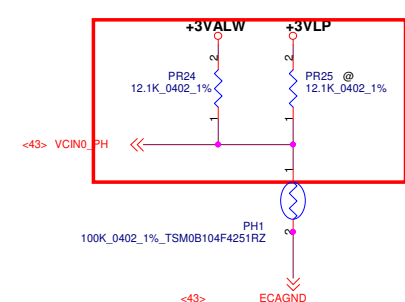
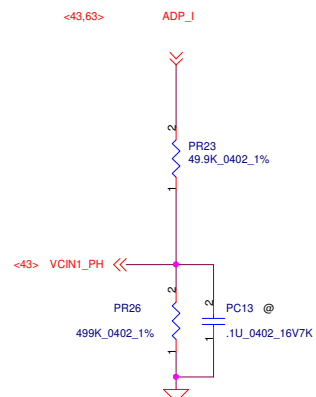


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Date	Friday, Jun 22, 2012		Sheet	53	of 61

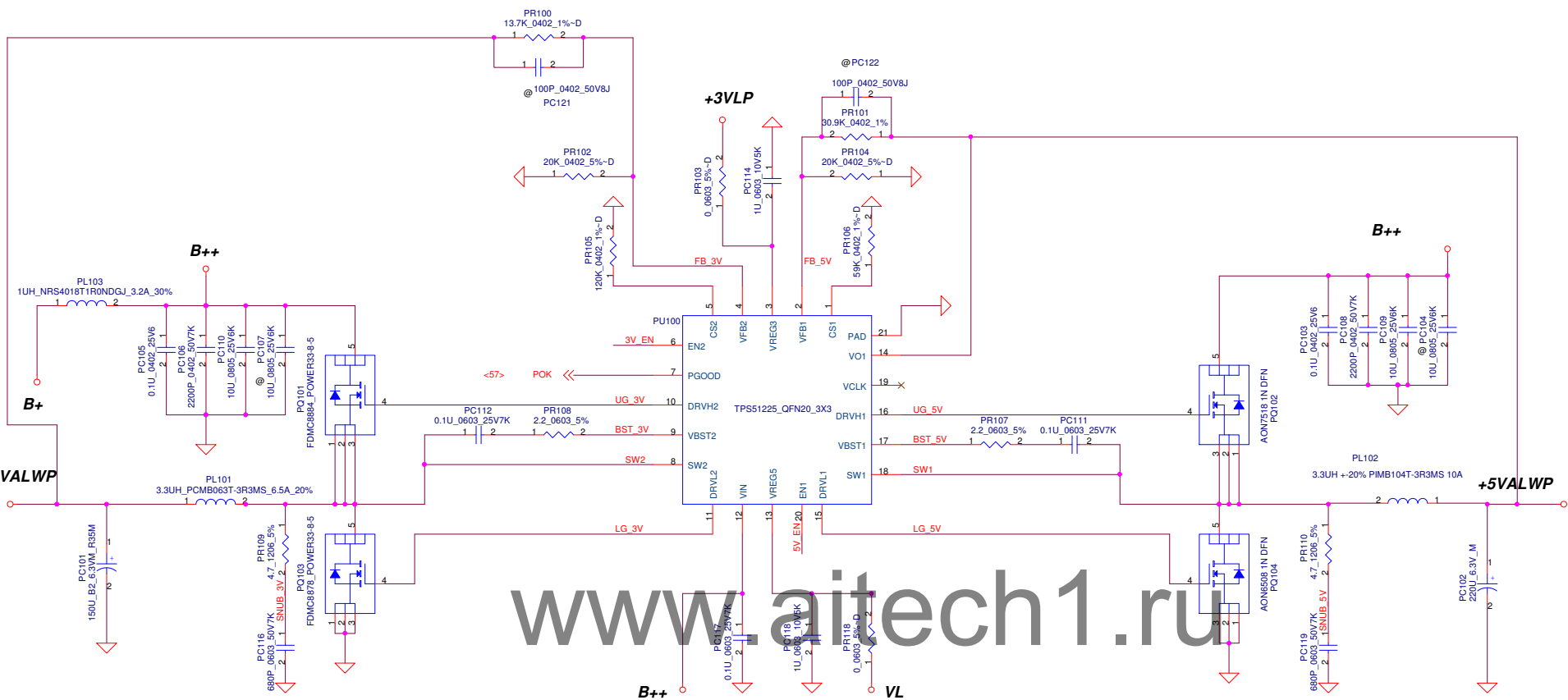


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PH1 under CPU bottom side :
CPU thermal protection at 93 +/- 3 degree C

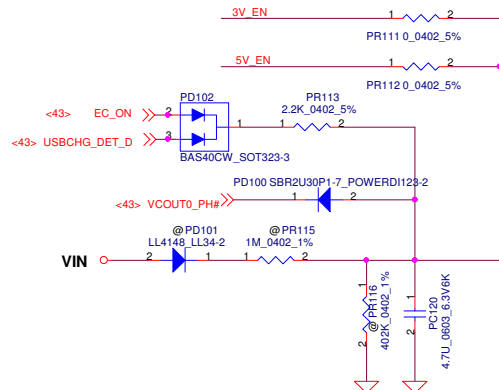


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				Rev	0.1
				Date:	Friday, June 22, 2012
				Sheet	54 of 61



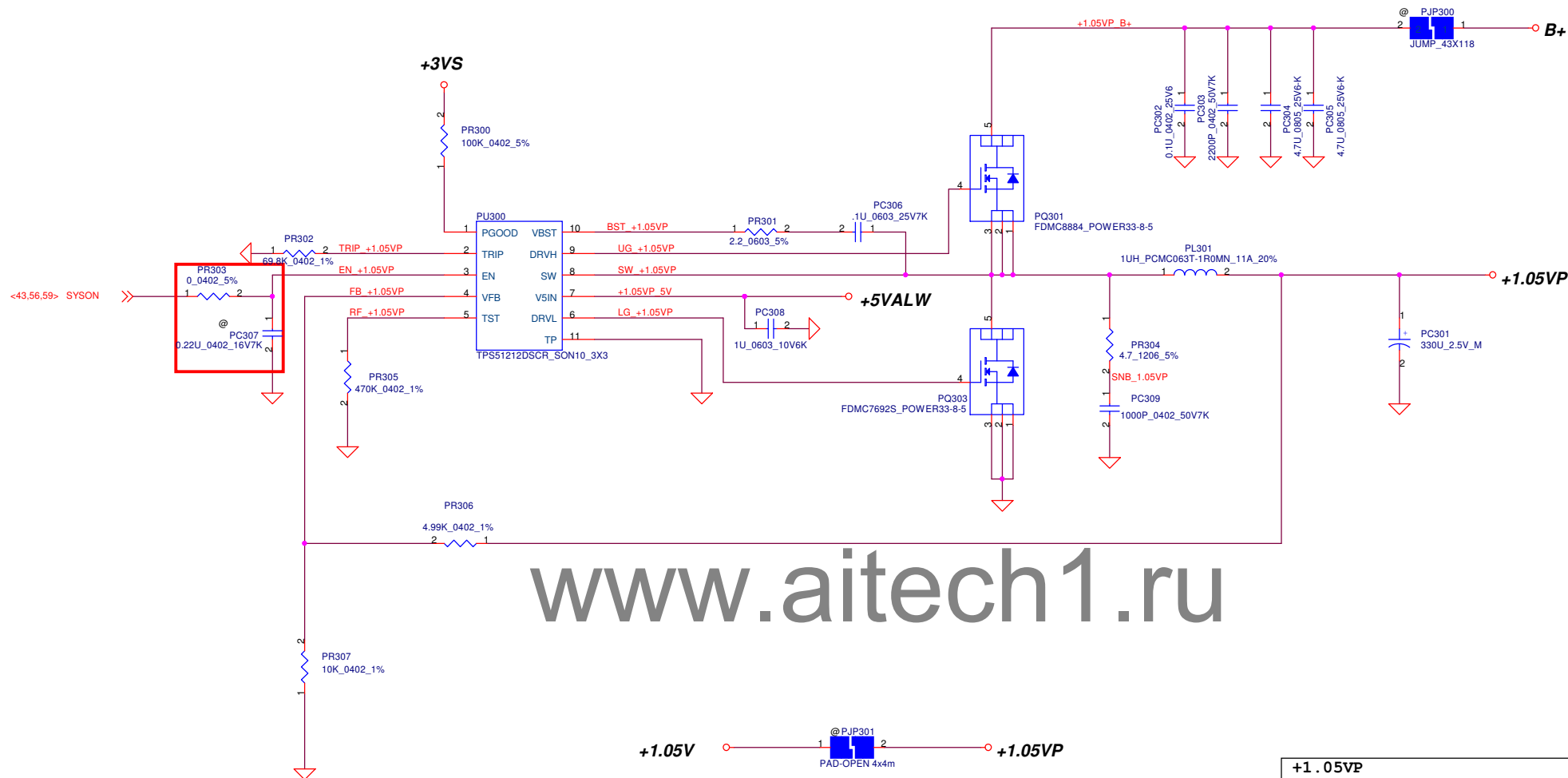
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3VALWP
TDC 6.08A
Peak Current 8.11A
OCP current 9.73A
TYP MAX
H/S Rds(on) :22mohm , 30mohm
L/S Rds(on) :12.1mohm ,17mohm



5VALWP
TDC 10.64A
Peak Current 14.19A
OCP current 17.03A
TYP MAX
H/S Rds(on) 11.2mohm , 14mohm
L/S Rds(on) :3.7mohm , 5mohm

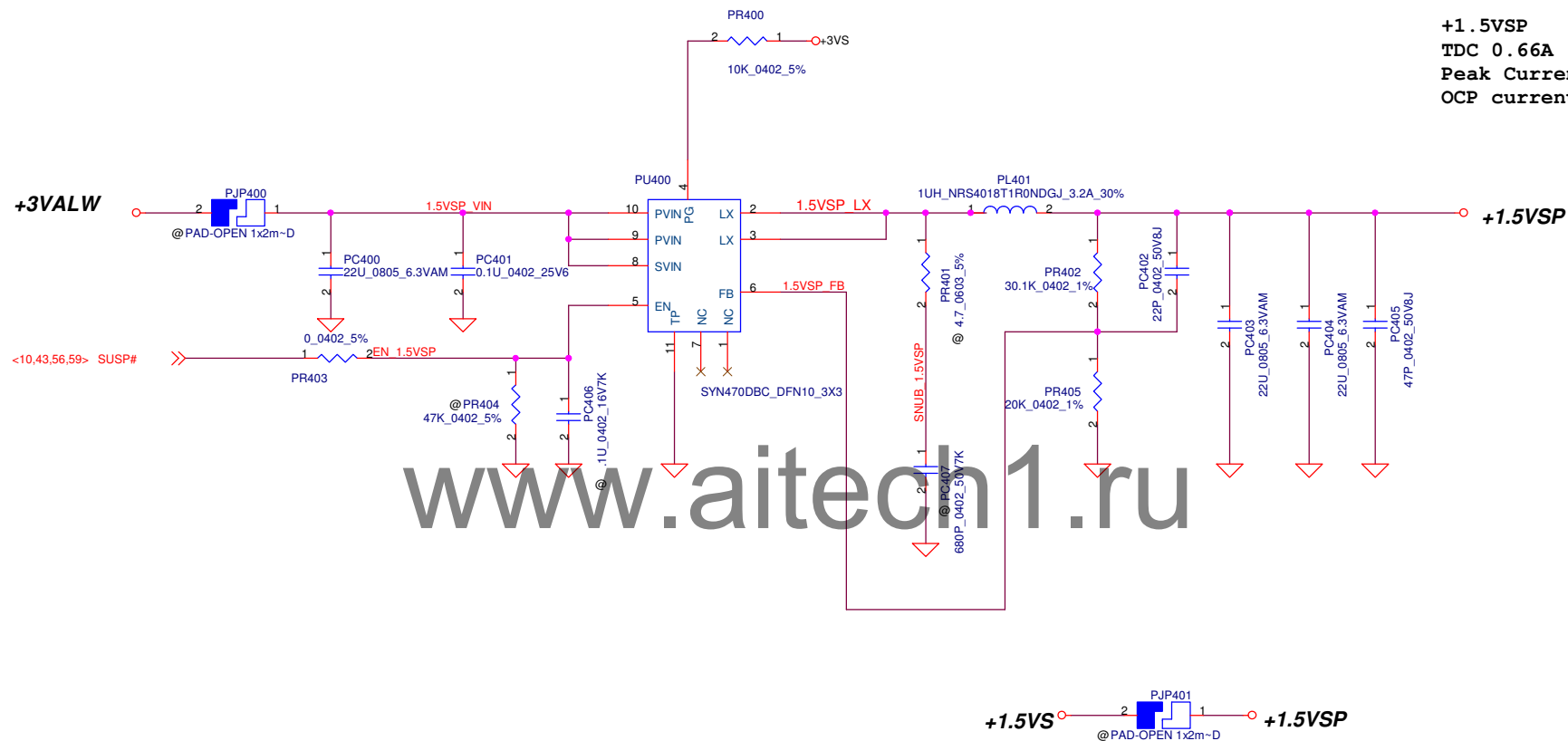
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				Date	Friday, June 22, 2012
				Sheet	55 of 61



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+1.05VP	
TDC 4.56A	
Peak Current 6.51A	
OCP current 7.81A	
	TYP MAX
H/S Rds (on)	:22mohm , 30mohm
L/S Rds (on)	:10.8mohm , 13.6mohm

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				Sheet	57 of 61
				Rev	0.1



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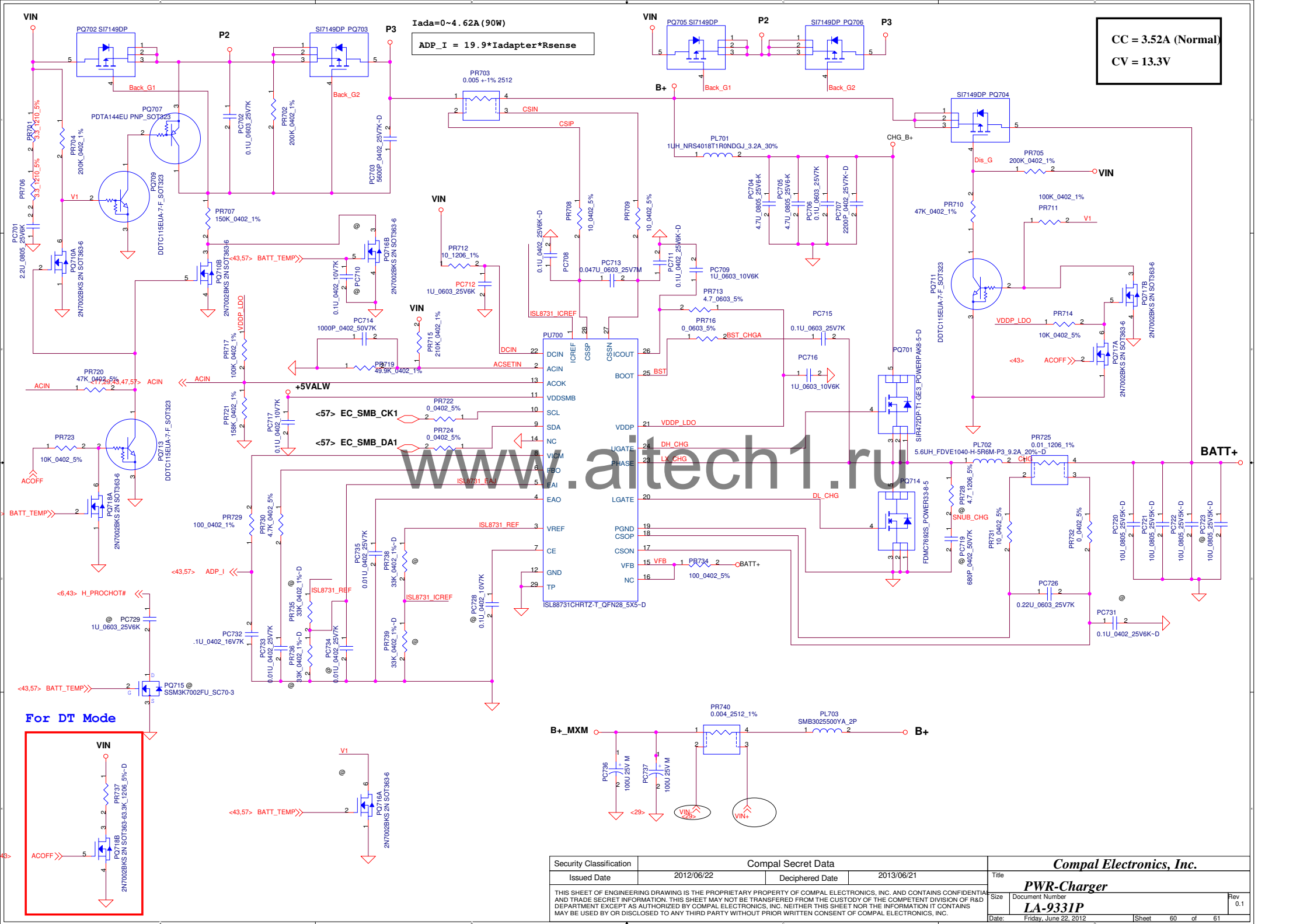
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Title			
PWR-1.5VSP			
Size	Document Number		Rev
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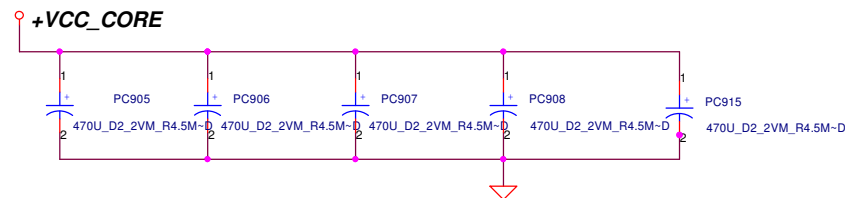
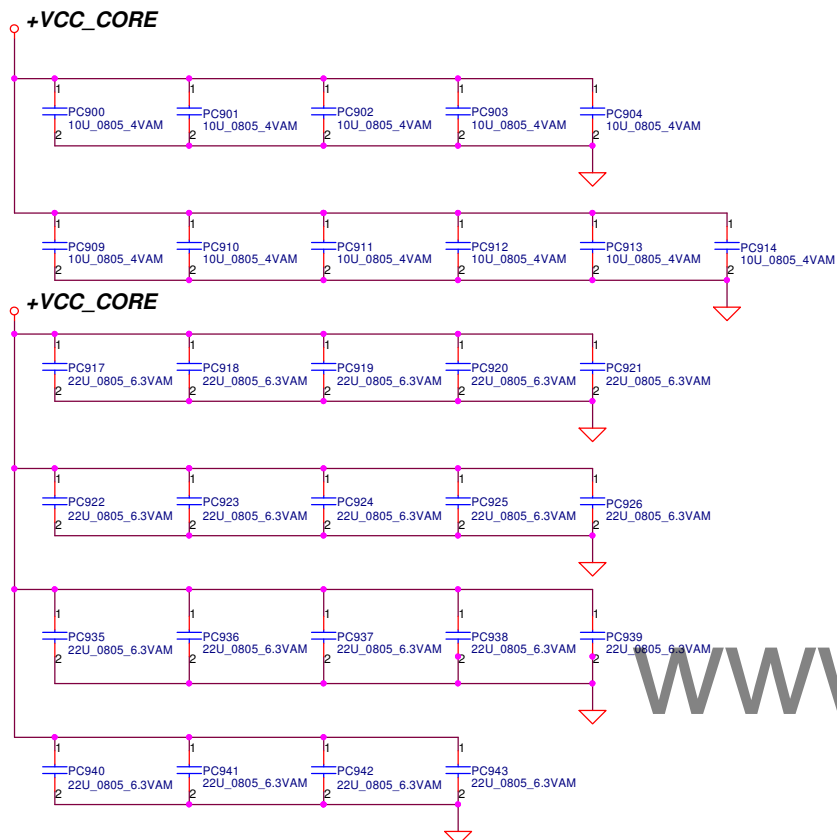


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	LA-9331P	0.1	
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Based on PDDG rev 0.8 Table 5-1.



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